# Protecting Legerity Subscriber Line Interface Circuits (SLICs) with Bourns® TISP® Protector Products

*Version 1*

BOURNS®

*Circuit Protection Solutions*

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# Objective

This engineering note provides a first principles theory and protection solutions when designing telecom circuit protection with Legerity's subscriber line interface circuits (SLICs). Protection against lightning disturbances is a key concern for increased reliability of the equipment and telecom standards conformance. This document should be used in conjunction with the SLIC data sheet and application notes to provide correct overvoltage interface to the SLIC.

SLICs covered in this document are intended to be protected with a battery tracking gated thyristor solution and covers trademark names such as the VoiceEdge™ and VoicePort™ product families.

***Note:*** *The high voltage TISP61089BD is discussed in this application note, but the design considerations discussed may also be used in other voltage options in the family.*

# Introduction to Legerity SLICs

## VE880 series VoicePort™

Legerity's tracking battery VoicePort™ VE880 series devices provide a highly functional line interface which meets the requirements of short and medium loop (up to 1500 ohms total) applications. The VE880 series integrates the CODEC and SLIC into a single package to provide direct interface into a digital backplane (PMI/PCM or GCI) solution. The VE880 series also includes a high voltage switching regulator, self-test, line test capabilities, integrated ringing (up to 140-Vpk), software programmability and a flexible signal generator with tone cadencing, caller ID generation and all BORSCHT functions for worldwide solutions.

## VE790 series VoiceEdge™

The VoiceEdge™ VE790 series includes quad and octal CODES and dual SLICs which when combined with the Bourns® protectors provide a complete software configuration to BORSCHT functions. The VE790 series also provides complete programmable control over subscriber line DC-feed characteristics such as current limit and DC template. These chips provide a programmable solution satisfying worldwide line card solutions by software configuration. The VE790 solutions include full GR844 compatible integrated line testing, programmable AC, DC and supervision parameters. The VE790 series offers integrated ringing up to 145 V peak or may also be used with external ringing configurations. The family also provides flexible signal generation with tone cadencing, caller ID and full worldwide programmability.

# Designing Protection Solutions

The circuit protection solution needs to be designed to ensure long-term reliability while also providing suitable protection to meet standards requirements. The protection solution is the first point of contact for electrical disturbances entering the line card. Design considerations such as selecting the right components, through ensuring correct layout can influence the performance and reliability of the protection circuit solution.

The overcurrent protector limits the current into the overvoltage protector and therefore needs to operate reliably under the calculated or proposed impulse currents. Coordination between the circuit protection components is key to helping to ensure the overvoltage protector does not fail prematurely. Overcurrent protectors that resistance changes under the electrical disturbance such as positive temperature coefficient (PTC) thermistors, need to also ensure that the standoff voltage rating of the component is also suitable. The change to a high resistance value can cause the generator test voltage to be developed across it.

### *Impulse waveforms*

Applications that require voltage coordination with the primary protector or where the secondary protection resets with the primary protector is desired in the application; a series resistance element such as a line feed resistor module or PTC thermistor may be considered. Coordination is covered on page 36 for GR-1089-CORE applications and page 38 for ITU-T recommendations.

The minimum current rating of the thyristor can be calculated using the following equation:

$$I_{PP} = \left( \frac{V_{GEN}}{R_{SERIES} + \left( \frac{V_{GEN}}{I_{PEAK}} \right)} \right)$$

Where $I_{PP}$ is the minimum rating of the thyristor, $V_{GEN}$ is the open circuit generator voltage and $I_{PEAK}$ is the peak short circuit current from the generator. $R_{SERIES}$ is the series resistance between the generator and the overvoltage protector.

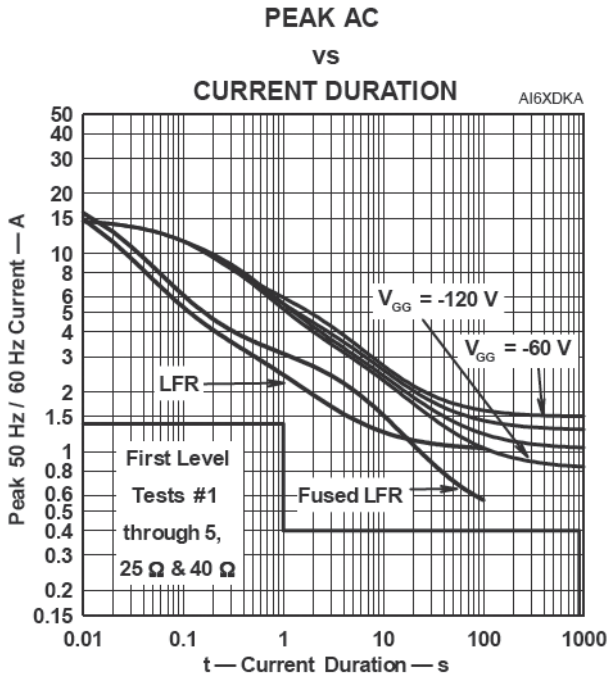
For example, Telcordia GR-1089-CORE specifies an intra-building first level 2/10 µs impulse with a voltage ($V_{GEN}$) of 1500 V and a short circuit current ($I_{PEAK}$) of 100 A. The impulse tester will therefore have a fictive impedance of 15 Ω (1500/100). Using a 6.5 Ω current limiter (MF-SM013/250) in series with the generator fictive impedance will reduce the thyristor current to 70 A ($I_{PP}$). Therefore, a thyristor rated lower than 100 A, but above 70 A 2/10 µs could be used to make the design as low cost as possible.

The standards may have repetitive tests where failure is not allowed and therefore time between tests needs to be considered as well. Resistor elements will dissipate power under the impulse tests where temperatures of the component could also rise where times between tests could have an effect on device performance and therefore reliability of the solution. The Bourns® TISP® thyristor is a semiconductor device with a low on-state voltage ($V_T$) to 3 V to limit power dissipation. The Bourns® TISP® device also does not have a wear-out mechanism provided the peak impulse currents are within the absolute maximum ratings and the junction temperature stays within the datasheet parameters.

***Note:*** *Impulse amplitude tolerances on the generator should also be taken into account.*

## *AC power contact calculations*

The circuit protection components are also subjected to AC tests to simulate power contact and induction conditions. There could be a fault condition where AC mains voltages are accidentally connected across the equipment terminals. Both the overvoltage and overcurrent components need to support the short circuit current tests. The gated Bourns® TISP® thyristor family specifies the peak non-recurring AC current vs. duration to aid correct design. The TISP61089BD absolute maximum peak rating is 4.6 A for 1 second or 0.73 A for 900 seconds (900 seconds can be considered continuous) using the EIA/ JESD51 environment and PCB layout (minimum copper and line interconnect) for the test.




***Graph 1** – Peak AC vs. current duration of the TISP61089BD and line feed resistor*

Telecom overcurrent resistance is normally limited to 50 Ω or less and therefore the additional series resistance in series with the AC generator resistance does not significantly impact the short circuit current levels through the Bourns® TISP® device. The important parameter is the time the overcurrent protector requires to operate. GR-1089-CORE second level AC power fault and UL 60950 allow the overcurrent protector to operate as a series fuse clearing to protect the circuit. The circuit protection solution needs to ensure the overcurrent protector will operate before the Bourns® TISP® device fails. To ensure this, the maximum current vs. time of the protectors needs to be known. Plotting both curves on the same graph will highlight if the protection components are suitable for each other. The Bourns® TISP® device curve should ideally be above the overcurrent protector curve as shown in Graph 1. If this is not the case, the thyristor could fail before the overcurrent protector operates.

GR-1089-CORE also specifies first level AC tests where the equipment must work as intended after the test. Therefore, the overcurrent protector must not operate or return to its original state under these tests. Graph 1 also shows the first level test criteria where the fuse characteristic should also be to the right of this curve to ensure conformance.

## *Maximum TIP and RING terminal ratings*

| | |
|---|---|
| Cont | VBH –1 V to BGND+1 V |
| 10 ms | VBH –5 V to BGND+5 V |
| 1 µs | VBH –10 V to BGND+10 V |
| 250 ns | VBH-15 V to BGND+15 V |

***Table 1** - SLIC absolute ratings*

Legerity SLICs are specified with an absolute maximum voltage rating with reference to the battery voltage(s) and ground. The SLIC absolute maximum withstand capability is also expressed in time to provide a protection envelope for the SLIC as shown in Table 1. This indicates that a gated thyristor protection solution is required since fixed voltage protection would allow at least 20 V of overstress to the IC under a continuous condition. This is due to the difference between $V_{DRM}$ (maximum normal working voltage) and $V_{(BO)}$ (thyristor crowbar voltage or protection voltage) specification. The positive maximum voltage of +/- 1 V is also referenced to the SLIC ground that highlights that a diode is required for positive voltage protection. The BGND+15 (BGND is the ground return for high and low battery supplies) highlights the forward voltage, VF requirement of the diode under fast impulse transients where a standard bridge rectifier diode may not suffice. The overvoltage protection ground connection has to be referenced to BGND to provide suitable protection.

***Note:** The electrical specification in Table 1 is derived from the Le79242 VoiceEdge™ data sheet. Please check maximum voltage ratings for your specific SLIC.*

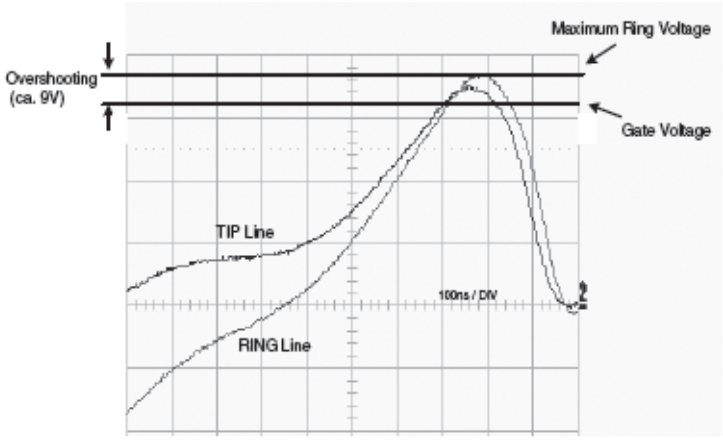
The maximum TIP and RING terminal ratings will vary over the wide ambient temperature range of the SLIC. The change of voltage rating per ambient temperature is standard for all semiconductors and therefore the thyristor protector will track the SLIC over temperature. This allows voltage definition of the protector to be initially done at 25 °C specifications. However, the junction temperatures between the SLIC and thyristor can differ under an AC fault condition, which needs to be considered. The $V_{(BO)}$ of the thyristor can vary by 7 % between junction temperatures of 25 °C to 150 °C and therefore this safety margin needs to be designed into the circuit protection solution.

The absolute maximum voltage differential between BGND and AGND (analog ground return for VCC) also needs to be considered. The Le79242 specifies an absolute maximum of ±3 V between these two grounds. The ground potential rise (GPR) of BGND under impulse should be considered where long track/wire lengths under fast current transients could easily exceed this specification if AGND and BGND are not referenced together. Good earth techniques (discussed on page 10) to reduce resistance and inductance between AGND, BGND and system earth need to be considered.

## *Limiting protection overshoots*

The impulse breakover voltage specification of the thyristor is dependent on the di/dt of the impulse waveform. Bourns specifies a maximum gate-cathode impulse breakover voltage, $V_{GK(BO)}$ to reflect situations under industry-standard waveforms. The $Q_{GS}$ of the gated thyristor also contributes to the overshoot value and is discussed in the gate decoupling capacitor section on page 8.

For example, the TISP61089BD is specified with a $V_{GK(BO)}$ of 12 V maximum with a 100 A 2/10 µs impulse. This has been tested with a $V_{GG}$ (gate-ground) of –100 V. This specification from the data sheet cannot be directly tied into the maximum terminal ratings of the SLIC since the length of time during the 12 V of overstress is not known.




Graph 2 shows the impulse breakover voltage of the TISP61089BD versus time. The impulse is 9 V above the battery voltage with a duration of 100 ns for the TISP61089BD with 100 A 2/10 µs at 25 °C. This protection is within the 250 ns, 15 V window specified for the SLIC.

***Graph 2** – Measured overshoot of TISP61089 gated thyristor*

***Note:** The overshoot of the thyristor is especially important when the SLIC is being operated close to its maximum supply voltage ratings.*

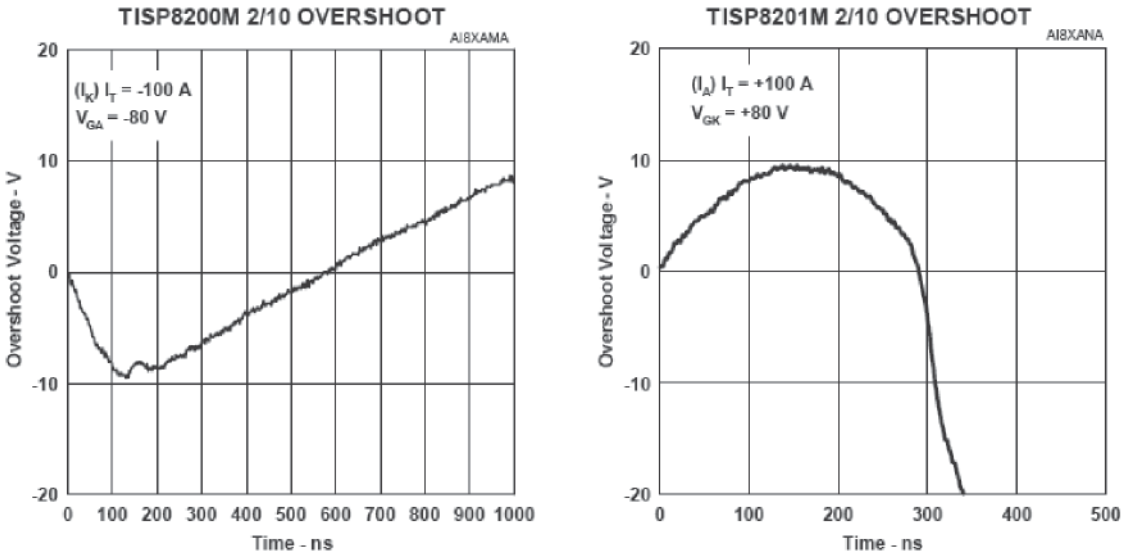
Increasing the line series resistor value has the effect of reducing the peak current into the thyristor and therefore the di/dt of the transient. A single blow fuse such as a Bourns® B0500T Telefuse™ Telecom fuse has low cold resistance value of 0.35 Ω. This provides fast di/dt conditions for the thyristor.

If increasing the line series resistance stops SLIC failure, the other area to consider is the ground connection between AGND and BGND and between the protector and the SLIC. This is discussed in “Grounding techniques” on page 10.

## Overshoot of the dual voltage TISP820xMD gated thyristors

The TISP8200MD and TISP8201MD dual voltage protectors are specified with a maximum impulse breakover voltage of 15 V under the 100 A 2/10 µs impulse. The typical overshoot impulse waveforms are shown in Graph 3. These can be used with the maximum voltage ratings of the SLIC to ensure suitable protection. The overshoot is also important when the overvoltage protection is operated close to the thyristor maximum $V_{RRM}$ (repetitive peak reverse voltage) value. With an absolute maximum rating of ±120 V, and 15 V of additional headroom to accommodate overshoot and variations with temperature operation, the maximum gate battery voltage should not exceed ±100 V on these devices.

***Note:*** *The integrated positive and negative TISP9110LDM has the same overshoot characteristics as the TISP820xMD series and therefore share the same design considerations.*



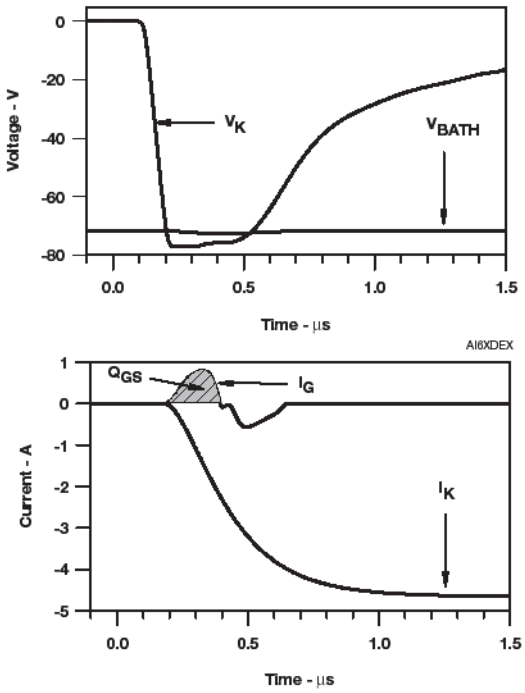

***Graph 3*** *– TISP820xMD overshoot characteristics*

The Le79252 dual voltage ringing SLIC has an absolute maximum $V_{BP}$ (positive battery) of +110 V and $V_{BH}$ (high battery supply) of –150 V with respect to AGND (analog ground for VCC return). At first glance, it appears that the TISP820xMD with a recommended maximum battery voltage of ±100 V would be unsuitable. However, the key parameter is the absolute maximum voltage rating between $V_{BP}$ with respect to $V_{BH}$. This is specified to be +160 V and highlights the maximum voltage differential for the SLIC. It is common to see $V_{BP}$ of +100 V and $V_{BH}$ of –48 V to keep the maximum differential voltage below 150 V.

The Le79252 specifies an envelope on its impulse ratings with respect to $V_{BH}$ and $V_{BP}$. From Graph 3, it can be seen that the overshoot does not exceed ±10 V and is within the ±15 V for 250 ns and ±10 V for the 1 µs requirement. It can also be seen that the ±5 V stress occurs in less than 350 ns providing excellent protection for this SLIC under the fast 100 A 2/10 µs impulse.

## *Gate decoupling capacitors*

Bourns® gated thyristor data sheets recommend a typical gate decoupling capacitor of 220 nF, but a minimum value of 100 nF may also be considered in the design. This capacitor is needed to ensure correct operation of the protector. During the initial rise of an impulse voltage, the gate current ($I_G$) is positive during approximately the first 20 % of the $I_K$ switch time as current is reflected into the gate from the cathode. The SCR gate then requires a negative drive current to switch the SCR into a low impedance condition. This equates into a positive and negative gate charge $Q_{GS}$ requirement. The required gate charge is supported with this capacitor to keep the overshoots to a minimum. For example, a 10 A/s rate of impulse current shows a positive gate charge of about 0.1 nC. For a 1 V battery voltage variation, this equates to 100 nF capacitor.




***Graph 4** – gated thyristor switch characteristics*

This is considered the minimum capacitance value in the data sheet for reliable operation with low overshoot properties. Reducing the value of this gate capacitor or eliminating it from the design will increase the overshoot of the thyristor. Faster di/dt impulses will also increase the $Q_{GS}$ of the gated thyristor and therefore the minimum value of gate decoupling capacitance should be selected for the worse case situation.

***Note:** The capacitor should also be placed as close as possible to the gate connector of the protector to minimize inductive effects of the copper tracking.*

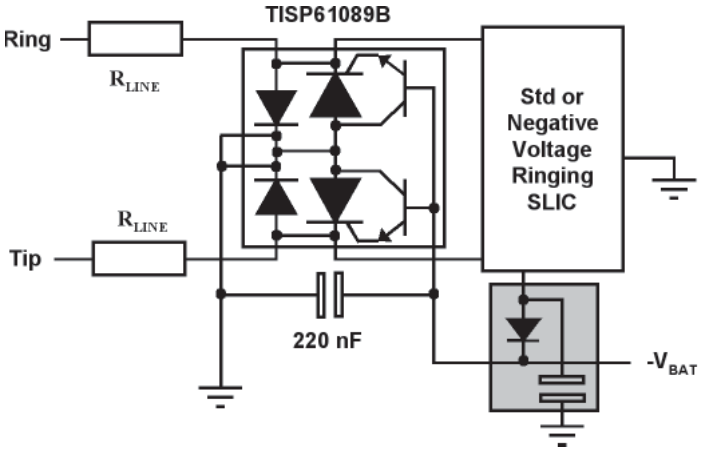
The negative battery voltage supply can be decoupled by a 100-220 nF capacitor from the dc/dc converter output to the SLIC. The Bourns® TISP® device gate decoupling capacitor can be used to provide the same function to save component cost if it is placed less than 1" (2.4 cm) from the dc/dc converter output. The gate decoupling capacitor still needs to be as close as possible to the gate of the thyristor to limit overshoots as discussed on page 10.

The NC (non-connect) pins on the TISP61089BD and TISP8200MD and TISP8201MD families are not connected to the die inside the package and therefore can be used to aid tracking. Pin 3 NC can be connected to pins 6 and 7 of the TISP61089BD to help place the decoupling capacitor next to pin 2 (gate pin) for example. Small size (1201) 100-220 nF capacitors are available that can utilize this interconnect layout across the package.

## $V_{BAT}$ power supply diode

The substrate potential for negative only SLICs must be the most negative pin; otherwise, the SLIC could latch-up or be permanently damaged.

A fast response (50 ns or less) diode as shown in Figure 1 is connected in series with the negative supply where it protects the SLIC against possible power supply reversal. The diode protects the SLIC against possible power supply reversal. This can occur during activities such as powering-up for example. Switch-mode power supplies have been specifically designed with low capacitor and ESR (effective series resistance) values on the output to ensure stability. Under normal operating conditions, this is not an issue, but under fast transient conditions, the $I_{GT}$ (gate trigger current) demand from the overvoltage protection could be high. Peak currents demanded from the gate can be as high as the current through the thyristor (with just a diode rather than a buffer transistor in place) for a very short period between 200-300 ns. The closed loop reaction time of the power supply may not be fast enough to react to this current demand. This in turn discharges the power supply capacitors and under extreme conditions where multiple circuit protection ports are operated together could make the negative battery power supply collapse or go positive and thus damage the SLIC. The buffered gate thyristor significantly reduces the chance of this problem occurring during the fault condition, as less current is demanded from the switch-mode power supply.




The power supply diode can be named differently in the SLIC family of data sheets, but resides between the high battery voltage ($V_{BH}$) of the SLIC and $V_{BATH}$ of the system. A lower specified recovery time diode could be used, but this increases the possible stress on the SLIC under the circuit protection operation.

***Note:*** *The $V_{BAT}$ power supply diode is a vital component in the operation of the SLIC where omission if required can affect its performance under surge. Please check the SLIC data sheet to aid selection of the diode to be used.*

***Figure 1*** *– Power supply diode and decoupling capacitor*

## SLIC decoupling capacitors

Legerity recommends using a decoupling capacitor as shown in Figure 1. If the SLIC fails impulse tests, the power supply decoupling capacitor can be placed between the cathode of the diode and ground instead. This will limit the energy stored in the capacitor discharging through the substrate of the SLIC if the TIP or RING is taken more negative than -Vbat.

This situation can occur under a fault condition where the protection circuit can let the line voltage go more negative than the battery voltage. If the capacitor is connected directly to the SLIC, the charge stored in the decoupling capacitor could still be discharged through the TIP or RING line if they are taken more negative with respect to $V_{BAT}$. The amount of charge will be dependent on the value of capacitor and battery voltage and could be enough to damage the SLIC if the capacitance value is increased from the data sheet specifications.

## *Grounding techniques*

PCB layout is critical to the performance of the protection circuit and can often be the culprit when the protection circuit does not work as intended. The gated thyristor's anode (ground) pins need to be connected as close as possible to the battery ground of the SLIC as shown in Figure 2. The gated protector's primary function is to limit the voltage stresses seen by the SLIC. Therefore, the gated thyristor needs to be referenced to the same ground as the SLIC to ensure minimum stresses. The current through the protector will be directed through the ground plane of the SLIC and therefore a suitable ground plane to support the expected current needs to be considered.

***Note:*** *The absolute maximum voltage rating highlighted in Table 1, page 5 indicates the ground of the gated thyristor needs to be directly connected to the SLIC ground pin. This point can also be called BGND and will be dependent on the SLIC used. Reference to the data sheet is required to ensure correct connection.*

Using short tracks between the gate of the thyristor and SLIC negative battery voltage is important where the resultant voltage caused by the current in the track will be added to the dynamic performance of the thyristor. Laboratory testing shows that during the initial rise, a fast impulse (80 A/µs) can cause inductive voltages of 0.8 V in 2.5 cm of the printed wiring track. This can be attributed to the inductance of the track where:

$$\left( V = L\frac{di}{dt} \right)$$

Designers sometimes have the protection circuit referenced directly to Earth on the equipment, rather than the SLIC ground point on the line card. The layout methodology is to divert the load current away from the system without the current going through the back plane of the equipment. Under standard resistance measurement, these two points look the same and therefore are not considered the problem area. However, the scenario is different under dynamic conditions. If a SLIC is failing under the fast transients (2/10 µs or 8/20 µs) but passes long duration impulses (10/1000 µs or 10/700 µs) it is a good indication that the problem may be grounding in the application.

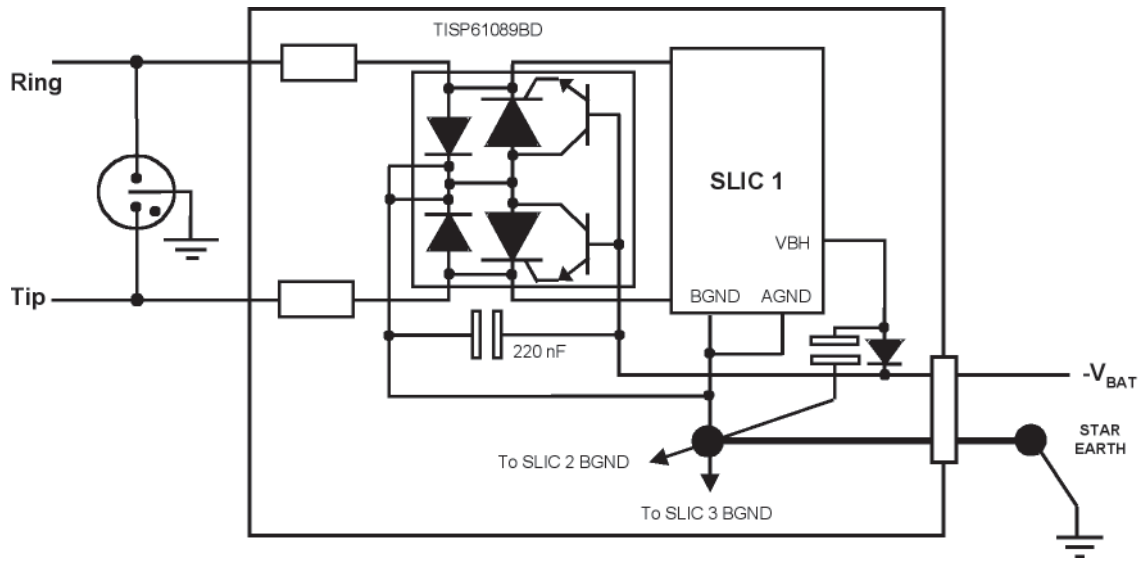



***Figure 2*** *– grounding techniques*

## *Specific Bourns® TISP® device design considerations*

Layout of the circuit protection components can also have an effect on circuit passing conformance. Telcordia GR-1089-CORE for example has a 2500 V, 500 A impulse test where a circuit protection solution using a 12.5 Ω line feed resistor will have at least 1786 V across the line interface terminals. Tracks that are routed close to the input pins can cause problems in circuit operation and the PCB isolation properties need to be considered for multi-layer boards.

## TISP61089BD 120 A 2/10 µs

The TISP61089BD has two K1 (TIP) connections specified as pins 1, 8 and two K2 (RING) pins 4, 5 of the SOIC 8-pin package. Each of these interconnects to the die have been designed to support the impulse and AC power cross of the device. Therefore, a layout that allows the TIP and RING lines to flow through the package is possible as shown in Figure 3. This adds another benefit in that the bond wires in the package can act as a "last resort" fuse that will isolate the line from the line card should the overcurrent protector not operate as intended. The line isolation will be at least 3.81 mm. This layout technique is not intended to remove the need for a suitable overcurrent protector, but to increase the level of safety should the overvoltage protector fail. It may also be considered where standards are not required such as customer premises equipment where port conductors do not leave the building (intra-building). This removes the need for additional overcurrent protectors to be used. Two ground pins (pins 6 and 7) are used to ensure a good ground return path and aid in dissipating heat away from the package under fault conditions.

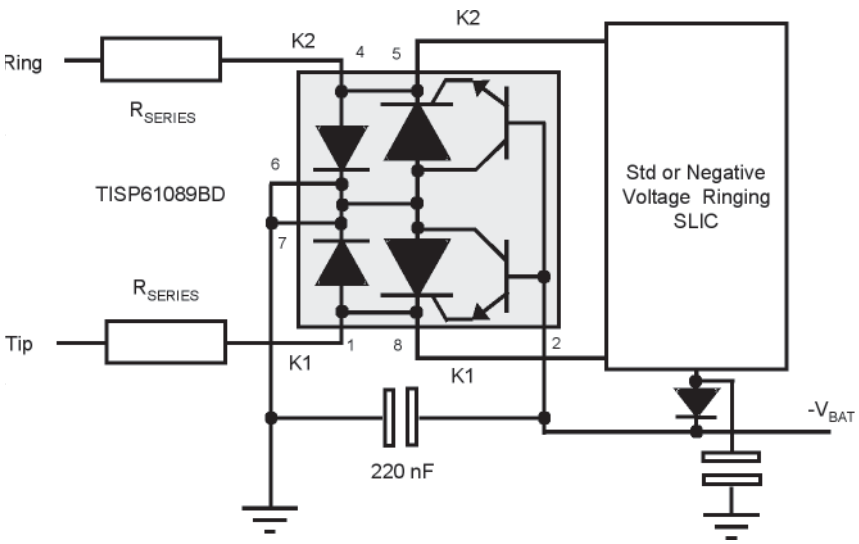



***Figure 3*** *– TISP61089BD K1 and K2 connection*

## Single blow fuses with the TISP61089BD gated thyristor

Single blow fuses are often considered as the overcurrent protector in telecom equipment. To ensure their suitability, the fuse should ideally open before the thyristor fails to ensure coordination between the two components (page 4, AC power contact). The 0.5 A B0500T fuse must only be used with the TISP61089BD, TISP820xMD and TISP9110LDM gated thyristor families. The 1.25 A B1250T fuse is unsuitable to be used with these gated thyristors.

The layout also needs to be considered since the B0500T is a slow-blow type specifically designed for telecom applications. In this instance, K1 and K2 pins should be connected in parallel as shown in Figure 4 to ensure adequate current carrying capability from the TISP61089BD. The coordination time of the B0500T and TISP61089BD family is very narrow where layout is especially important in this configuration. The minimum pad area for the fuse should be used to aid heating of the fuse and the Bourns® TISP® device ground connection should be as large as possible to aid power dissipation.

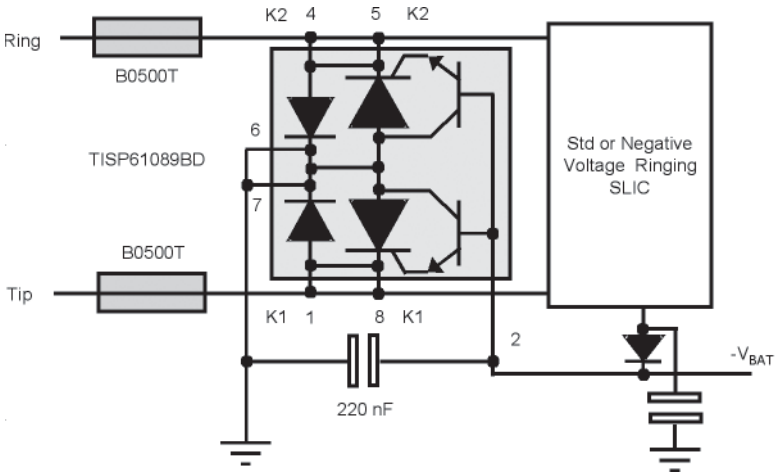
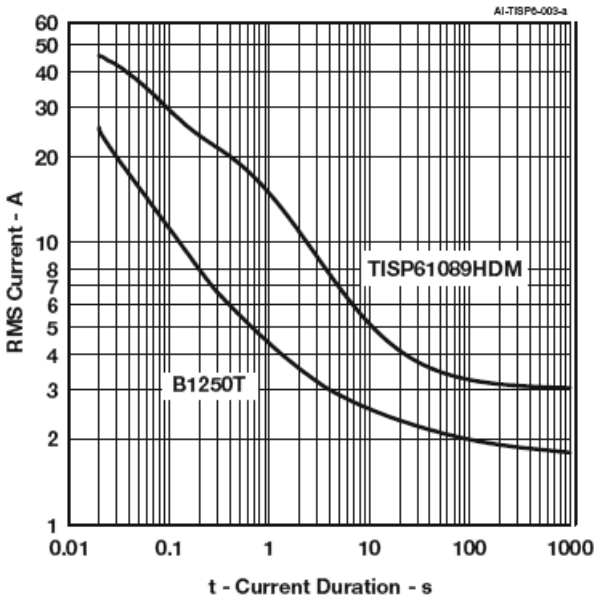



***Figure 4*** *– TISP61089BD connection when using the B0500T fuse*

***Note:*** *The 1.25 A B1250T fuse should not be used with the TISP61089xD, TISP820xMD or TISP9110LDM families.*

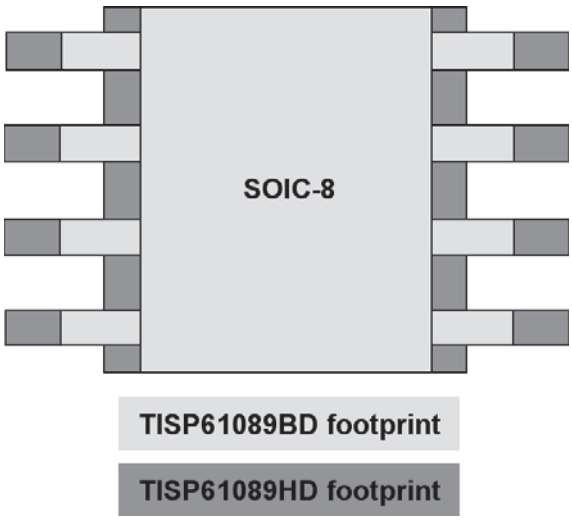
## TISP61089HDM 500 A 2/10 µs

The integrated single port 500 A 2/10 µs TISP61089HD has been integrated in the wide-body SOIC 8-pin package. The lead frame in the package has been designed to be a heatsink and therefore as much copper for the connections should be used for the board layout. This is especially important for the ground pins (pins 6 and 7) that connect directly to the die. K1 (and K2) pins need to be connected together to ensure the TISP61089HD coordinates correctly with the Bourns® 1.25 A B1250T Telefuse™ Telecom fuse. The TISP61089HDM is rated to pass the first level AC tests in GR-1089-CORE.




GR-1089-CORE second level AC tests allow the equipment to fail, but not to cause a hazard such as fire or fragmentation. Figure 5 shows the typical time for the B1250T fuse to open compared to where the package will sustain damage. Plotting the non-repetitive peak on-state current versus the current duration curve highlighted in the data sheet indicates the B1250T will clear before the TISP61089HDM fails short to help ensure the application fails open circuit.

***Figure 5*** *– Typical time to open versus current*




The 100 A TISP61089HDM gated thyristor now allows a single platform to be designed to support the lower current TISP61089BD option since the pin pitch and pin function is exactly the same for both devices. This allows a single board design capable of supporting all regions around the world, while capitalizing on the cost advantages in packaging and die sizes between the two devices. Figure 6 highlights the overlay between the standard SOIC and wide-body SOIC package.

***Figure 6*** *– TISP61089BD and TISP61089HDM PCB layout consideration*

TISP61089HDM also requires a small diode plus two resistors (1 Ω and 1 kΩ) component network to help ensure that the device is stable at extended (above 150 °C absolute maximum datasheet rated specification) junction temperatures. The buffer transistor can go into an intrinsic short under extended (250 °C) junction temperatures that could short the battery supply to ground. This circuit can be used to drive multiple gates of the TISP61089HDM as shown in Figure 7.

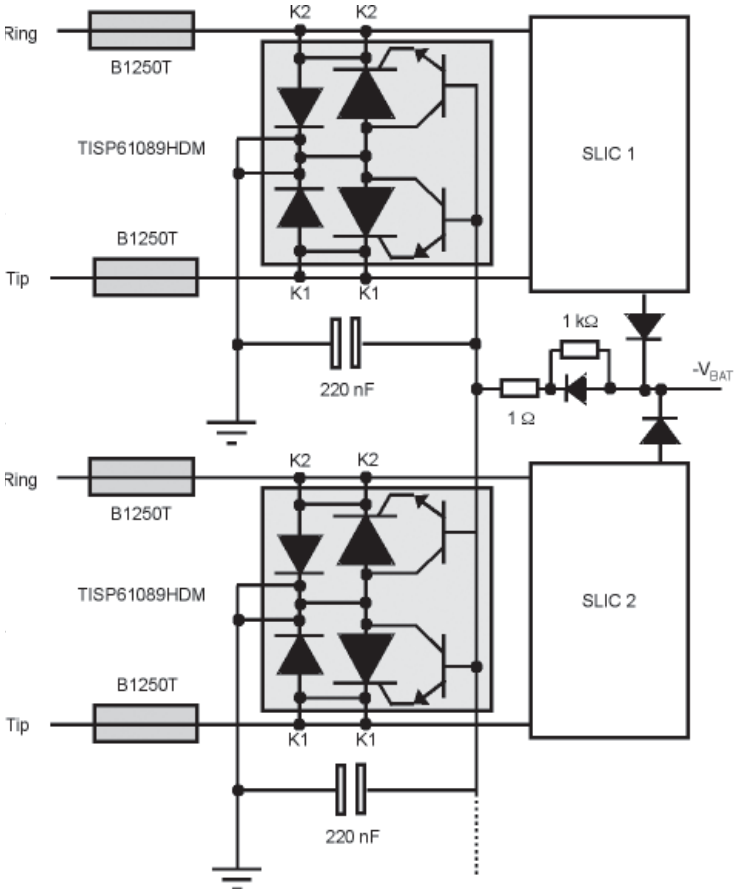
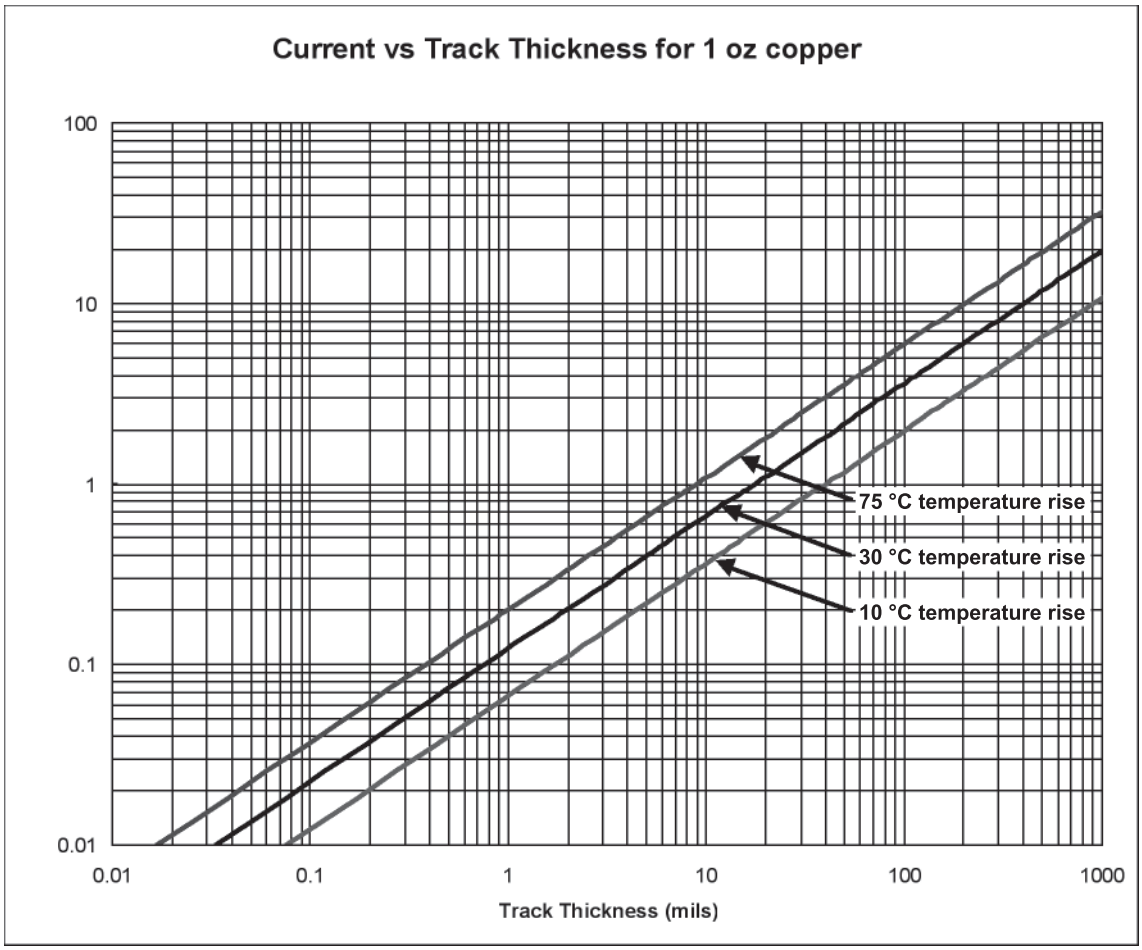



***Figure 7** – TISP61089HDM dual SLIC layout*

## *Track thickness for the circuit protection*

The ground connection of the thyristor needs to be dimensioned to support the current from the electrical disturbance from impulse and AC power contact tests. This has to be done from the TIP/RING lines on the edge connector to the backplane edge connector. The backplane to Earth in the rack mount also needs to be considered. The standard method to calculate track thickness uses the IPC-D-275 model that specifies the trace widths versus current handling capabilities with track temperature rise. These calculations are for continuous current handling capabilities where Graph 5 shows the load current verses the required track thickness with a 10 °C, 30 °C and 75 °C temperature rise. Telecom fuses have long clearing times under the 2.2 A, 900 s test and therefore, this graph highlights that a 0.045 ” thickness should be used with 1 oz copper. This can be reduced to 0.025 ” if the track temperature can increase by 75 °C.




***Graph 5*** *– IPC-D-275 current vs. track thickness recommendation*

***Note:*** *A common design trace width of 0.035 ” with 1 oz copper is often used to meet Telcordia GR-1089-CORE applications.*

## *Maximum battery voltage*

The maximum supply voltage of the SLIC will define which buffered gated thyristor is best suited to the application. The Bourns® gated thyristors are specified with an absolute maximum repetitive peak gate-cathode voltage, $V_{GKRM}$ specification. The TISP61089BD maximum $V_{GKRM}$ rating of –167 V does not indicate that a maximum of –167 V battery voltage can be used as the gate reference voltage. The dynamic performance of the device needs to be taken into account to ensure the thyristor voltage rating is not exceeded. The TISP61089BD has a maximum gate-cathode impulse breakover voltage and a $V_{GK(BO)}$ rating of 12 V with 100 A 2/10 µs impulse. With a 120 A rating and to take into account extended temperature operation, 15-20 V should be considered in the design. This increase in protection voltage is covered in more detail in the IEEE Std C62.37.1-2000, IEEE Guide for the Application of Thyristor Surge Protection Devices. Therefore, the TISP61089BD should only be used for battery supplies up to –150 V. Table 2 highlights the impulse and $V_{GKRM}$ rating of the popular gated thyristor family.

| Device | 2/10 µs / 10/1000 µs current rating | $V_{GKRM}$ | Suggested $V_{BAT(MAX)}$ | Comments |
|---|---|---|---|---|
| **Single Negative Voltage SLICs** | | | | |
| TISP61089DR | 120 A / 30 A | -85 V | -60 V | $T_J$ = -40 °C to +85 °C |
| TISP61089ADR<br>TISP61089ASDR | 120 A / 30 A | -120 V | -100 V | $T_J$ = -40 °C to +85 °C |
| TISP61089BDR | 120 A / 30 A | -167 V | -150 V | $T_J$ = -40 °C to +85 °C |
| TISP61089HDMR | 500 A / 100 A | -167 V | -150 V | $T_A$ = 25 °C |
| TISP6NTP2ADR | 85 A / 20 A | -90 V | -70V | $T_J$ = -40 °C to +85 °C |
| TISP6NTP2CDR | 90 A / 20 A | -167 V | -150 V | $T_J$ = 0 °C to +70 °C |
| **Dual Voltage Ringing SLICs** | | | | |
| TISP8200MDR<br>TISP8201MDR | 210 A / 45 A | ±120 V | ±100 V | $T_J$ = -40 °C to +85 °C<br>$V_{GKRM}$ at $T_A$ = 25 °C |
| TISP8210MDR<br>TISP8211MDR | 167 A / 60 A | ±120 V | ±100 V | $T_A$ = 25 °C |
| TISP9110LMDR | 100 A / 30 A | ±120 V | ±100 V | $T_A$ = 25 °C |

***Table 2** – TISP® impulse vs. absolute maximum gate-cathode voltage*

# TIP and RING overcurrent protection options

SLICs have traditionally required line resistance with a tight ratio-matched (0.5 %) tolerance to ensure stability line balance. This resistance is becoming less important with SLICs where line compensation is built in as an added feature. For example, the VE880 series monitors the line current and varies the line voltage according to the loop current. This also helps to lower the average power dissipation of the SLIC. For overcurrent protectors such as line feed resistors (LFRs), this allows the ratio matching of the line resistors to be less of a concern where a 5 % and ratio-matched tolerance is possible.

## *Single blow fuses*

Single blow fuses induce the highest di/dt transients in the gated thyristor and therefore extra caution needs to be used in the design. Fuses open with a function of localized heat where the fusing characteristics can change with board layout. The recommended footprints highlighted in the datasheet should be used to ensure correct operation. The fuse characteristics can also change with excessive soldering temperatures that can anneal the fuse wire to change its characteristics. The 1.25 A B1250T and 0.5 A B0500T fuses are RoHS compliant and have been designed for the high reflow characteristics associated with the process. Hand soldering of components using high tip temperatures with extended times needs special precaution and should be avoided.

To calculate the suitability of the fuse under impulse test conditions, the following formula can be used for impulse decay waveforms of 10 ms or less -

$$I^2t = 0.72 \bullet {I_{PP}}^2 \bullet t_D$$

where $I^2t$ is the rating of the fuse, $I_{PP}$ is the peak current and the $t_D$ is the decay time in seconds of the impulse waveform.

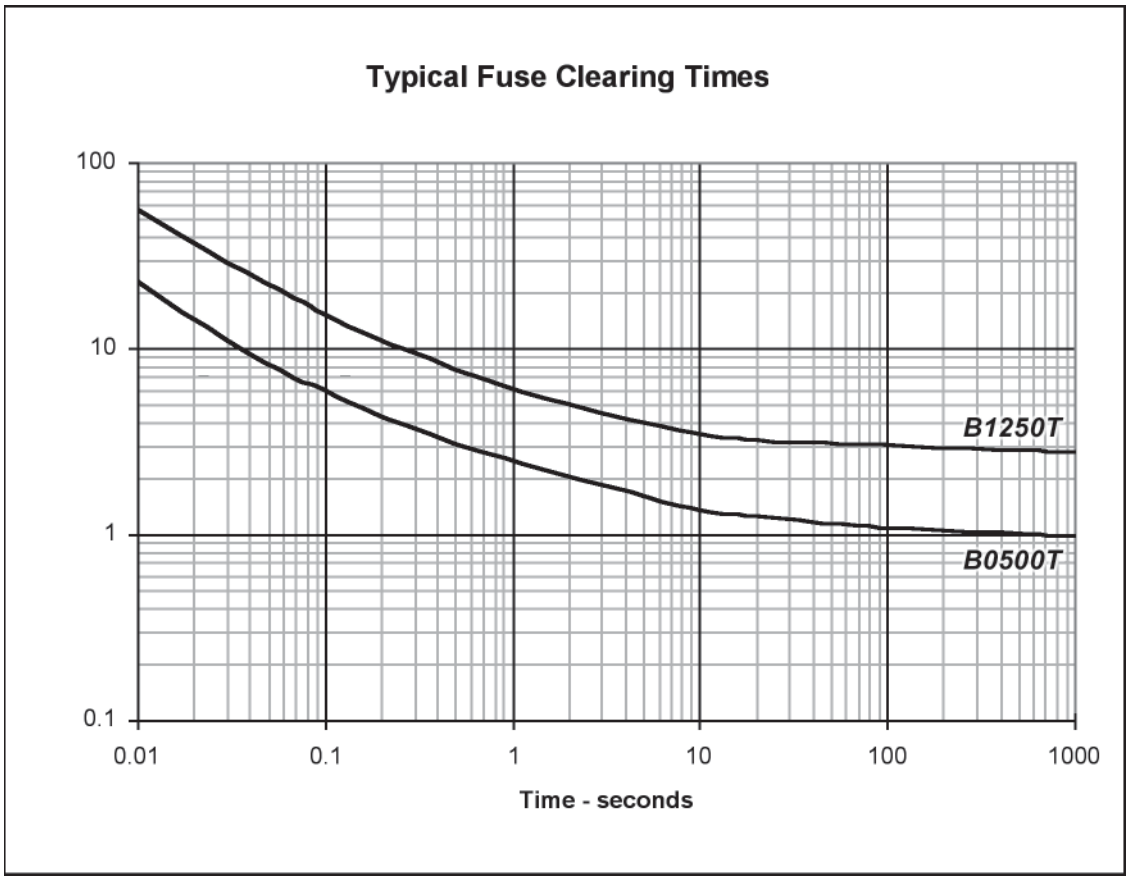
For example, what $I^2t$ rating will be suitable for GR-1089-CORE first level 100 A 10/1000 µs impulse?

The $I^2t$ of 7.2 is the absolute minimum rating required since GR-1089-CORE also specifies an amplitude tolerance of 0 % to +15 % and a duration of 0 µs to +500 µs. Putting the new values of 115 A and 0.0015 s into the equation, the $I^2t$ rating has to be 14. The B1250T fuse is specified for an $I^2t$ of 14 and therefore ideal for GR-1089-CORE applications.

***Note:*** *Waveform tolerances in amplitude and wave shape decay times may be specified in the requirements and should be taken into account if the equipment must operate after the tests.*

## Clearing time under AC

Calculating the clearing time of a fuse under AC conditions is difficult to do given the wide tolerances. The simplest method is to use the characterized curves where Graph 6 shows the Bourns® B1250T and B0500T clearing times under AC test conditions. The Bourns® TISP® device thyristor AC withstand capability can also be plotted on the curve to help ensure its suitability with the overcurrent protector. The fuse curve should ideally be below the thyristor curve to ensure the fuse operates before the thyristor fails.




***Graph 6** – AC clearing times*

## *Line Feed Resistors (LFRs)*

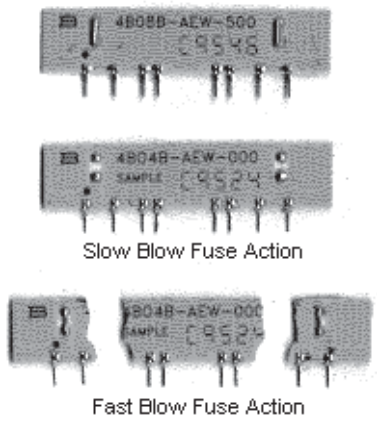
Series resistance required between the SLIC and the telephone line is dependent on the SLIC and therefore should be checked in the data sheet. For example, the Le79242 call these resistors $R_{FAi}$ and $R_{FBi}$ with a value of 50 Ω and 2 % tolerance.

***Note:*** *The manufacturer's data sheet should be consulted to identify the correct resistance value for the SLIC.*

There are two resistor tolerances to consider with LFRs. The resistance tolerance is the variation from one resistor to another resistor between two different devices. Tolerance between the resistors on a single device is called the ratio-matched tolerance and aids longitudinal balance where long loop lengths are being used. Bourns® LFR modules specify the resistance tolerance that can be specified down to ±1 %, but ±5 % is a common tolerance to be used. The LFR module data sheets also specify a ratio-matched tolerance specification down to ±0.5 % where ±1 % is the standard tolerance. Bourns® LFR modules also offer very low resistance variation over temperature where the data sheets often specify the resistance tolerance to include a wide ambient temperature range of -40 °C to +85 °C to address remote access units.

Bourns® LFR modules are manufactured by depositing (screening) high precious metal content resistive inks onto a ceramic substrate to create the required resistance. The resistance values are laser trimmed to the required tolerances in the final stages of production. The LFR module has been designed to withstand the high-energy impulse content of telecom surges and the AC power line cross tests. An important design consideration is that the resistance value will not vary significantly in its electrical characteristics under the telecom tests or over temperature. The high precious metal content in the ink helps ensure the resistance is stable under these conditions.

Many Bourns® LFR modules incorporate thermal fuses to protect the module against excessively high ceramic temperatures. Should the module temperature rise significantly, the fuse link will melt and reflow to the solder pads. This will open the communication line and effectively isolate the line card from the fault. The ceramic temperature can be in the region of 165 °C or more before the thermal fuse opens. The performance of the thermal fuse can be specified as watts dissipated versus clearing time and are often shown in a graph to aid the design engineer.



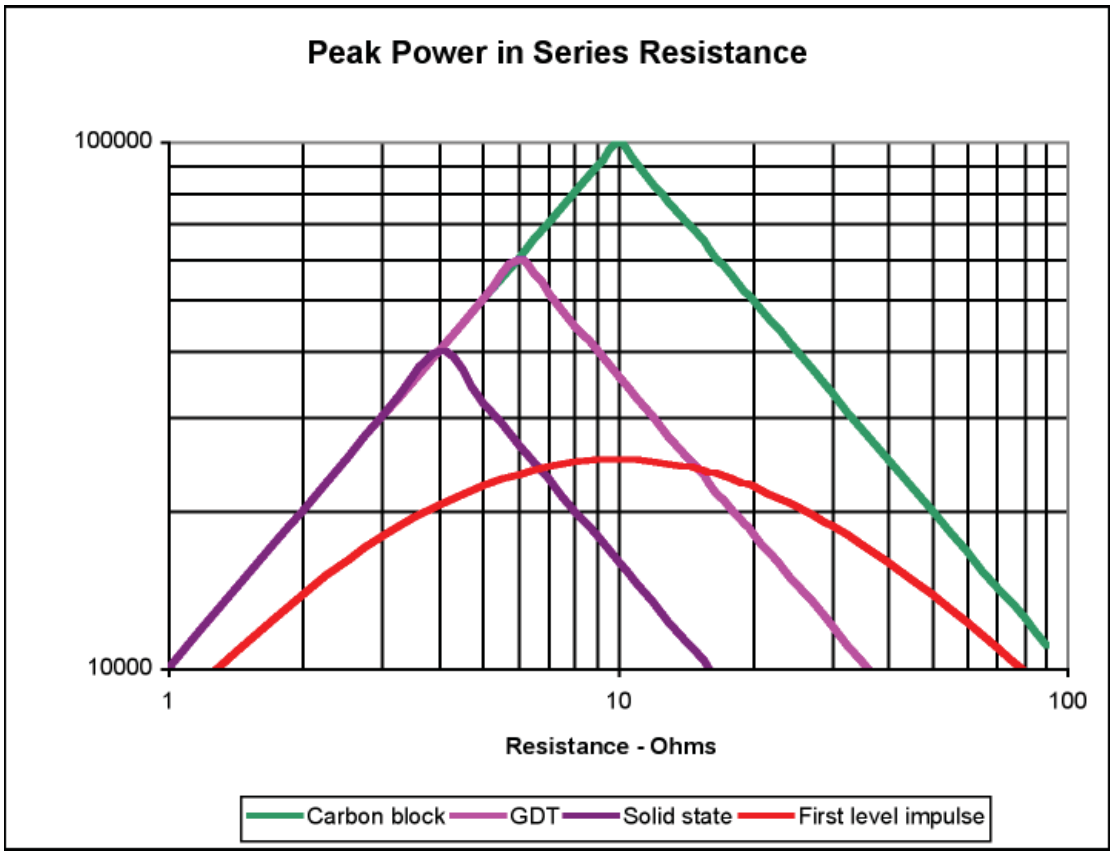

***Note:*** *The thermal fuse on the LFR module must not be used as a telecom current operated fuse.*

The ceramic substrate has also been designed to cleanly crack in one or more places during high-energy faults such as the 60 A, 5 second test under GR-1089-CORE tests for example. A key design consideration is for the ceramic not to fragment under this clearing method and to help ensure the crack distance is wide enough to limit arcing across the break. These two clearing modes are shown in Figure 8.

***Figure 8*** *– LFR clearing options*

### *Power dissipation in the LFR*

Defining the primary protector to be either a GDT or solid-state primary protector can also provide lower stress on the secondary protection circuit. For example, $R_{SERIES}$ of 10 Ω, without the primary protector specified will see a peak power of 100 kW under GR-1089-CORE, Issue 3 coordination testing. A defined GDT for the primary protector will reduce the peak power to 36 kW as shown in Graph 7. The peak power under the first level impulse is used to highlight issue 2 requirements. It can be seen that the power dissipation requirement for the resistor has significantly increased. The sweet spot is where the resistor dissipates the same energy under Issue 3 so that the size of the LFR does not need to change for this test. Graph 7 highlights a sweet spot for the coordination resistance of 15 Ω when a GDT primary and a 6.5 Ω solid-state primary protector are used. Reducing the resistance from these values increases the power dissipation requirement of the series resistor compared to the old GR-1089-CORE, Issue 2 requirements. Reducing the resistance will increase the size and cost of the ceramic resistor to withstand the impulse test.



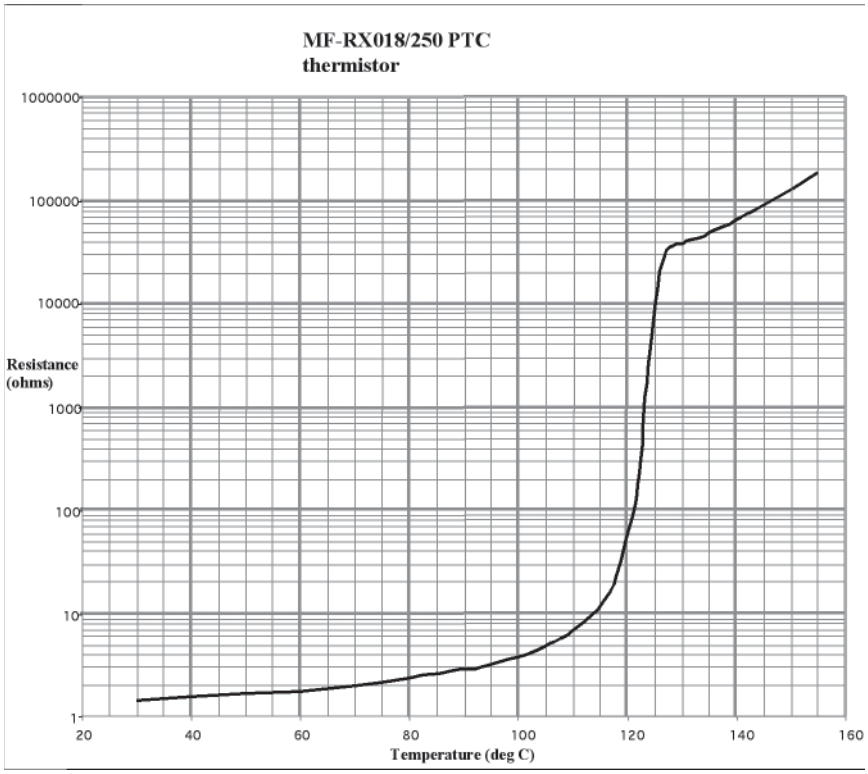

***Graph 7** – Power dissipation in series resistor under GR-1089-CORE coordination tests*

Graph 7 highlights the benefit of increasing the series resistance to reduce the power dissipation in the secondary protection, but the first level AC power fault tests highlighted in Table 4, page 33 also need to be considered. The highest power dissipation in the series resistor is achieved with the 3 A, 1.1 second test which may cause the thermal fuse to operate. Tests have shown that the LFR resistance should be 10 Ω to 15 Ω to keep the size and cost of the ceramic to an acceptable level. Bourns® latest GR-1089-CORE Issue 3 LFRs must also be specified with a GDT defined as the primary protector for the equipment to pass the new coordination test. The time delay between the repetitive first level AC tests (page 32) must be long enough to let the ceramic temperature return to ambient temperature to limit the compounding temperature rise that could prematurely activate the thermal fuse. A test delay time of at least 15 minutes is recommended for the first level GR-1089-CORE AC tests with the 4A12P-1AH-12R5 module.

***Note:** GR-1089-CORE, Issue 3 compliant modules need a GDT specified as the equipment primary protector.*

## *Positive Temperature Coefficient (PTC) thermistor*

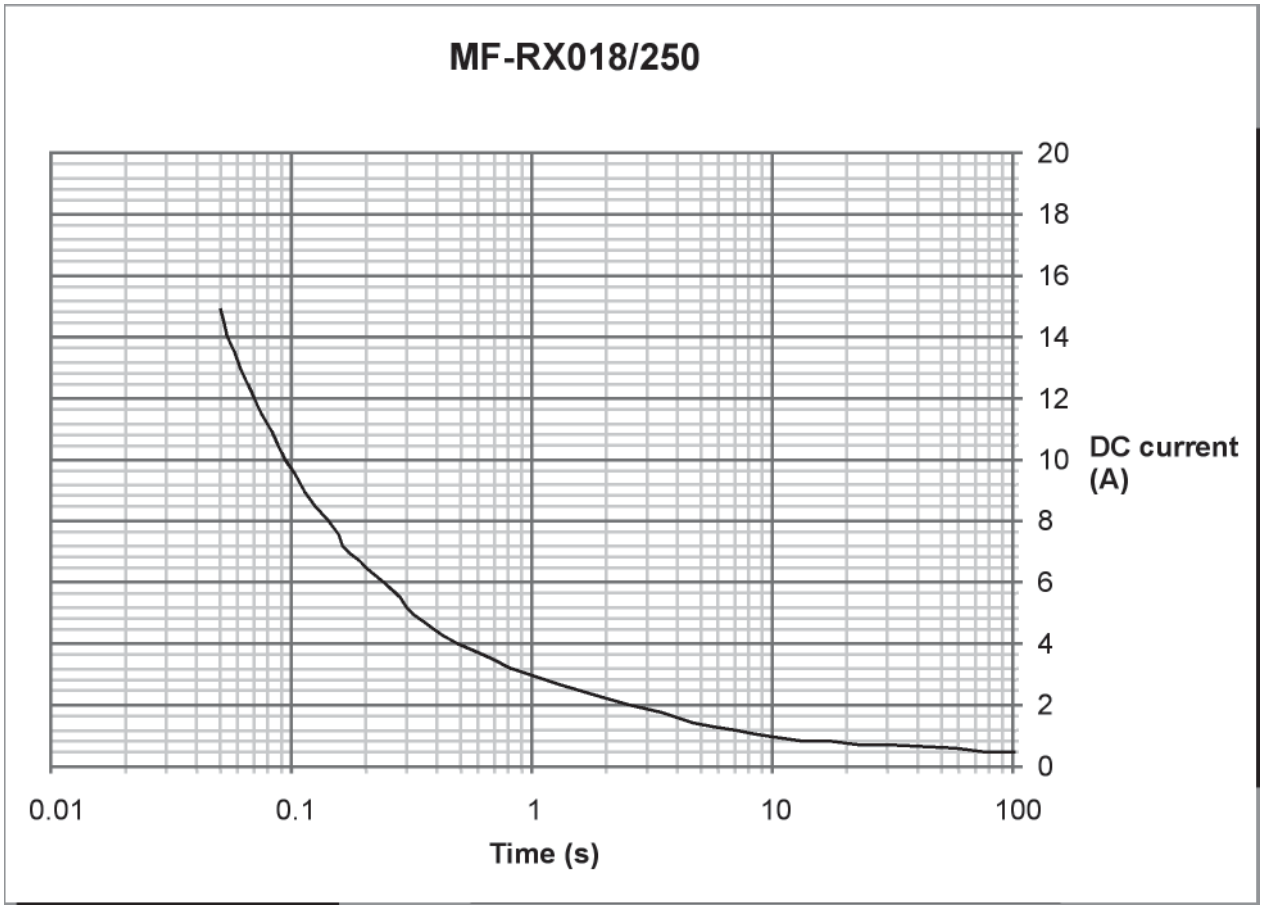
Positive temperature coefficient (PTC) thermistor's resistance increases with its increase in body temperature. The load current through the resistor causes a heating effect ($I^2R$) where the PTC resistance will significantly increase at a certain temperature. This threshold can be in the region of 85 °C to 135 °C depending on the polymer compound material used. A typical resistance verses temperature curve is shown in Graph 8.




***Graph 8** – MF-RX018/250 PTC resistance vs. temperature*

The trip resistance of the PTC thermistor increases four to five orders of magnitude more than the original resistance and will take time to reset back to its nominal value. Bourns® MF-RX018/250 specifies a one-hour post trip resistance of 4 Ω from the initial maximum resistance of 2 Ω. The hold current ($I_{HOLD}$) is the minimum current the PTC will conduct without tripping at the maximum rated continuous voltage ($V_{max}$). This parameter is usually specified at room temperature where an increase in ambient temperature results in a reduced trip current. For example, the MF-RX018/250 $I_{HOLD}$ value will reduce by 24 % from an ambient temperature of 23 °C to 50 °C. This needs to be considered in the design phase to help ensure the PTC does not trip at normal extended temperature operation of the equipment.

The trip current ($I_{TRIP}$) is the current at which the PTC trips at the given $V_{MAX}$ specification. A PTC can go into its high resistance state anywhere between $I_{HOLD}$ and the trip current ($I_{TRIP}$) and is largely dependent on the PTC resistance value. The PTC will stay in its tripped state until the load current falls below its new tripped $I_{HOLD}$ value. The holding current will be extremely low due to the elevated package temperature and therefore manual reset of the system may be required. The $I_{TRIP}$ value is normally 2x $I_{HOLD}$ value when calculating the extended ambient temperatures. As the PTC trip is dependent upon current, there is a relationship between trip time and current. Low fault currents close to the trip current specification can exhibit long delay switch times as shown in Graph 9, which should also be considered.




***Graph 9*** *– trip time vs. DC current for the MF-RX018/250*

Telecom PTCs specify a maximum rated continuous dc voltage ($V_{max}$) that needs to be specified to the maximum battery voltage. The critical area to consider PTC suitability is under the ring cycle at extended temperatures. A PTC with a lower series resistance or higher holding current may be required. The maximum interrupt voltage ($V_{int}$) rating is the maximum voltage that can be applied across the device while in the temporary tripped state and will often be specified with a maximum current specification. The interrupt voltage specification is expressed in AC rms for telecom applications since the PTC will protect against the AC test voltage conditions in the telecom standards. Therefore, it is prudent to ensure the PTC can support the maximum AC voltage (120 V rms, 230 V rms or 600 V rms) and withstand short circuit currents indicated in the telecom standards without being damaged.

***Note:*** *Ceramic PTCs (CPTC) typically display higher resistances (50 Ω), but the actual value of resistance can reduce by 50 % under high voltage and/ current impulse conditions. This needs to be taken into account when calculating the overvoltage impulse current requirements. Polymer PTC thermistors do not exhibit this negative resistance change and calculations can be done on the lowest ambient temperature specification.*

# Application solutions for negative only battery supplies

### *Telcordia GR-1089-CORE, Issue 3 inter-building requirements*

Telcordia GR-1089-CORE impulse requires a first level test of 100 A 10/1000 µs and 500 A 2/10 µs where the equipment must operate after the tests. Therefore, the overvoltage protection solution should be rated to at least these current levels if a single blow fuse is used. Bourns® TISP61089HDM is rated for these impulse capabilities and therefore the Bourns® B1250T Telefuse™ Telecom fuse can be used as shown in Figure 9.

The B1250T is designed to meet the surge withstand ratings with the quantity of repetitions in the data sheet. The B1250T must not open under the first level AC power contact tests while failing safely under the second level tests. The B1250T specifies the clearing time under the key AC current test conditions. It is considered good design practice to ensure the overcurrent protector operates before the overvoltage protector fails. This is not specified in Issue 3, but with a fuse in series, it is suitably coordinated with the overvoltage protector to help ensure that the equipment fails open circuit rather than the overvoltage failing short circuit without the fuse operating.

The equipment is also subjected to a current limit test where a current limiter indicator such as a MDL2.0A fuse is used between the generator and the equipment. The equipment must limit the current so that the current limiter indicator does not operate. The B1250T will help ensure that this requirement is achieved. The TISP61089HDM with the B1250T provides a simple method to help pass the coordination test in Issue 3.

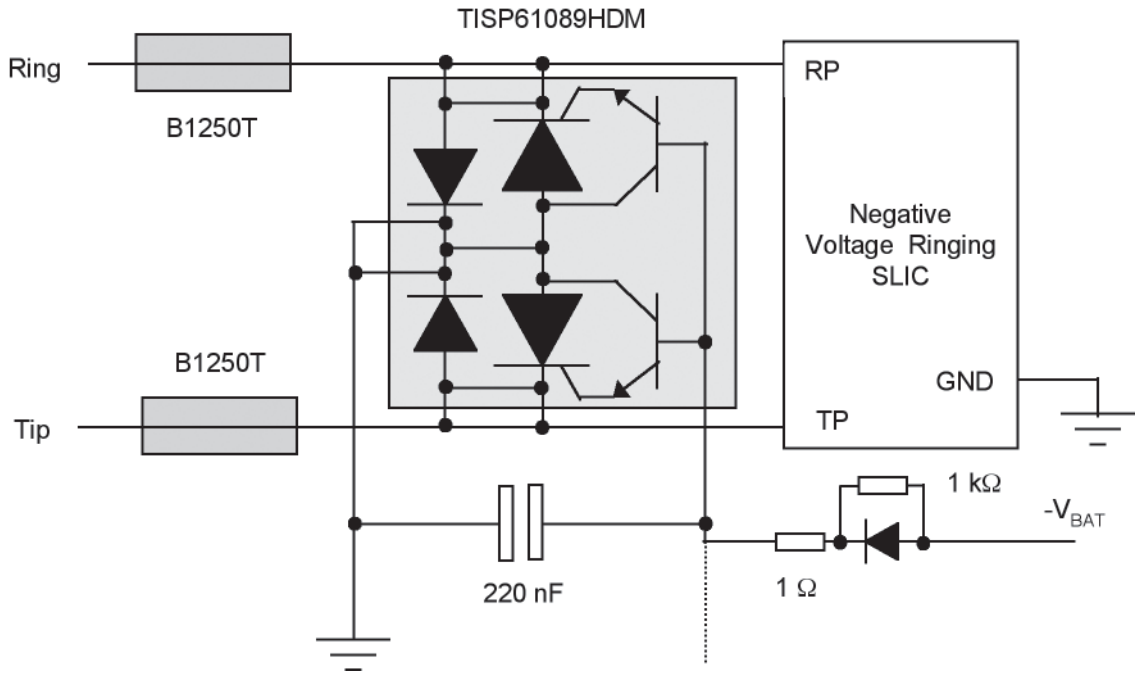



***Figure 9*** *– Telcordia GR-1089-CORE, Issue 3 protection solution*

Solutions that deploy the primary protector close to the secondary protection can find the single blow fuse failing before the primary operates.This is due to not having any series resistance between the two (primary and secondary) overvoltage protectors. The secondary is normally lower in voltage operation and therefore will operate before the primary protector and consume the entire fault current until enough voltage is developed across the primary protector. The simplest method to ensure this voltage coordination is to add series resistance where enough voltage is developed across the resistor (without failure) to operate the primary protector and allow the secondary protection to reset back into its normal condition. A fuse will need to operate before this can be achieved if there is not enough interconnect impedance (inductance or resistance) between the two elements to create the voltage. The 4A12P-1AH-12R5, 12.5 Ω LFR module helps ensure voltage coordination (Telcordia GR-1089-CORE, Issue 3, section 4.6.7.1 type A pass) between the primary and secondary protection. A minimum impulse current rating of 51 A, 10/1000 µs is required to meet coordination. A solution is shown in Figure 10. Should the series resistance increase to 40 Ω or higher, the lower impulse rated TISP61089BD can be considered in the design.

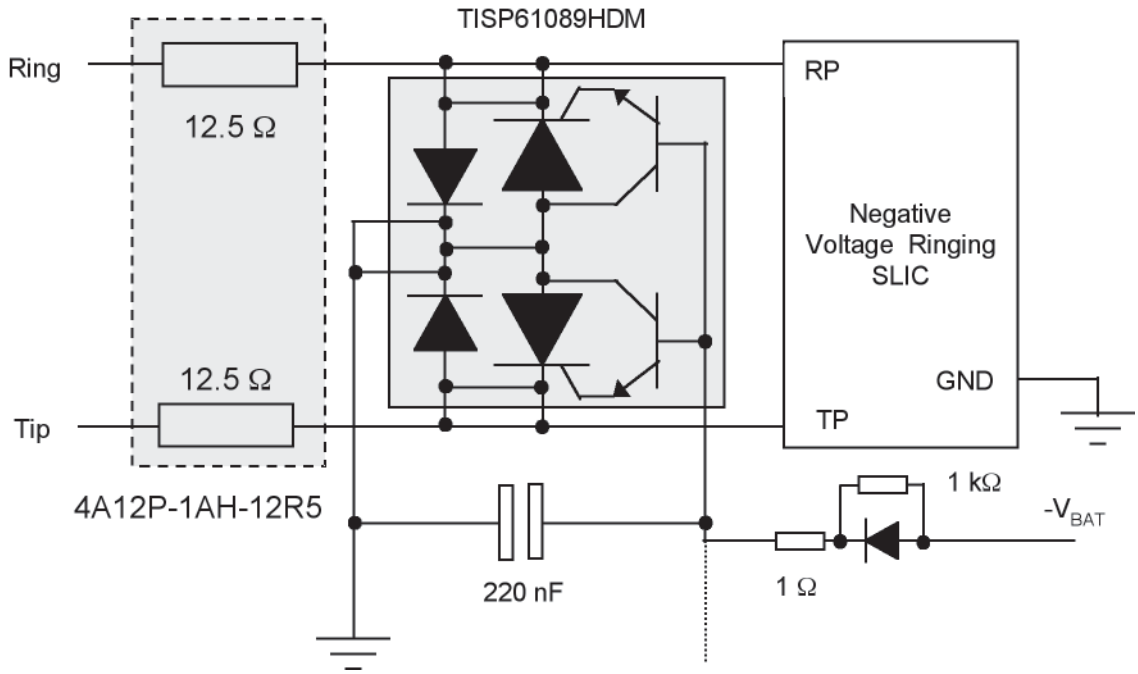



***Figure 10*** *– GR-1089-CORE voltage coordination protection*

***Note:*** *The Bourns® MF-R015/600 and MF-R016/600 devices are unsuitable for full Telcordia GR-1089-CORE applications. It is also important to ensure the selected LFR module conforms to the latest standards.*

## *USA intra-building recommendations*

Customer premises equipment (CPE) communication ports that do not leave the building do not have any circuit protection regulations. Equipment manufacturers recognize that equipment still needs to be protected to reduce field failure returns. Using just the TISP® overvoltage protector increases the system withstand to impulse condition or engineers can consider the Telcordia GR-1089-CORE intra-building requirements.

This requirement is for internal (within the building) communication ports within the central office and is a good indication of electrical disturbances occurring inside the building. GR-1089-CORE intra-building is covered in more detail in appendix A, page 32.

GR-1089-CORE intra-building has a 100 A 2/10 µs test where the equipment must work after the test. The TISP61089BD has a 120 A, 2/10 µs capability that ensures intra-building impulse requirements are achieved without the need of additional series resistance. Intra-building also has a 120 V rms, 25A test where the equipment can fail safely. The TISP61089BD will need to be protected against the AC power line contact test since it can support 0.93 A for 900 seconds. The B0500T current versus time characteristic shows that it will operate before the maximum withstand of the TISP61089BD is exceeded. K1, (pins 1 and 8) and K2 (pins 4 and 8) may be linked on the PCB if the 0.5 A B0500T fuse is used. For applications that require the overcurrent protector to reset, the Bourns® MF-RX018/250 or MF-SM013/250 Polymer PTC thermistor can also be considered in the design that can withstand the impulse and AC tests. A solution for intra-building is shown in Figure 11.

***Note:*** *The 1.25 A B1250T fuse is unsuitable to be used with the TISP61089BD thyristor.*

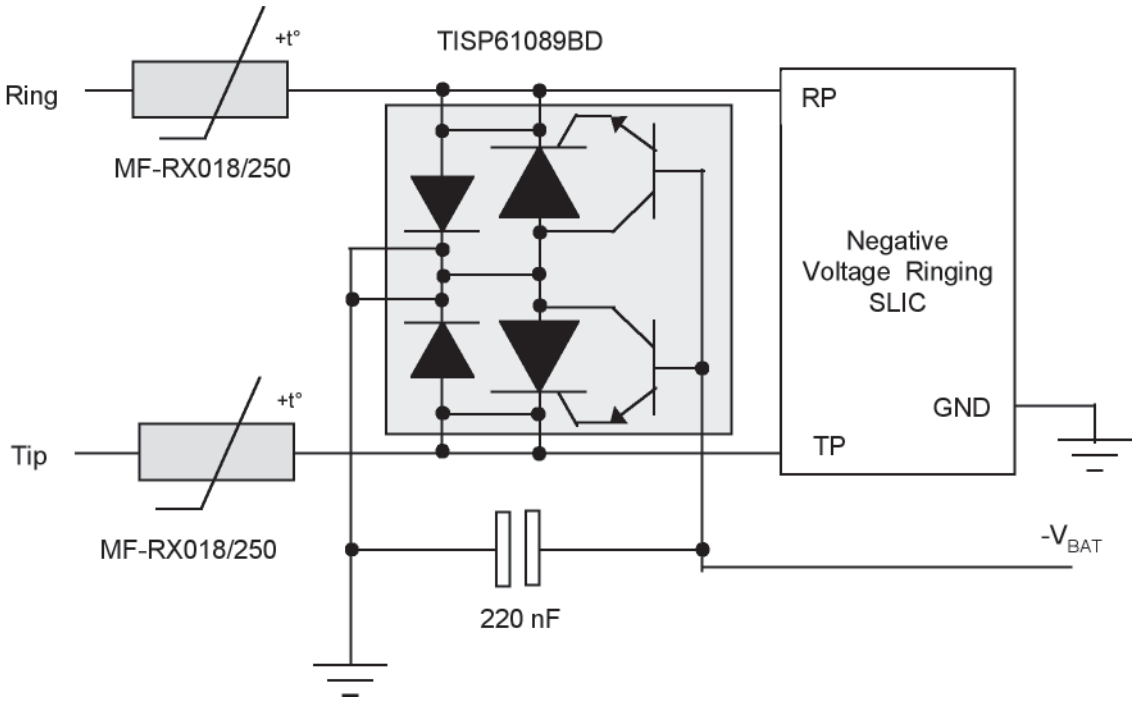



***Figure 11*** *– GR-1089-CORE intra-building requirements*

***Note:*** *Intra-building is not a requirement for CPE equipment and therefore the TISP61089BD layout considerations using the internal bond wires as a 'last resort' fuse as discussed on page 11. This can save the cost of using an overcurrent protector if thyristor failure is acceptable.*

## Dual or multiport protection for Telcordia GR-1089-CORE intra-building

For applications that have two or more POTS (plain old telephone service) ports for intra-building, the TISP6NTP2CD and the MF-SM013/250 PTC thermistor can be considered as shown in Figure 12. The TISP6NTP2CD integrates the function of two TISP61089BDs into a single SOIC 8-pin package to save space. The TISP6NTP2CD is rated for 90 A, 2/10 µs and therefore will require a minimum series resistance of 2 Ω or greater to pass the Telcordia intra-building impulse requirements. The MF-SM013/250-2 has a minimum of 6.5 Ω and has 250 V rms maximum interrupt voltage to withstand the AC test. The MF-SM013/250V provides a vertical PTC to help further reduce board space area. The Bourns® Multifuse® PTC device resistance can be 0.5 Ω reel-matched for better longitudinal balance if required.

***Note:*** *The TISP6NTP2CD should only be used with the MF-SM013/250 family or 50 Ω ceramic PTCs to meet the intra-building requirements.*

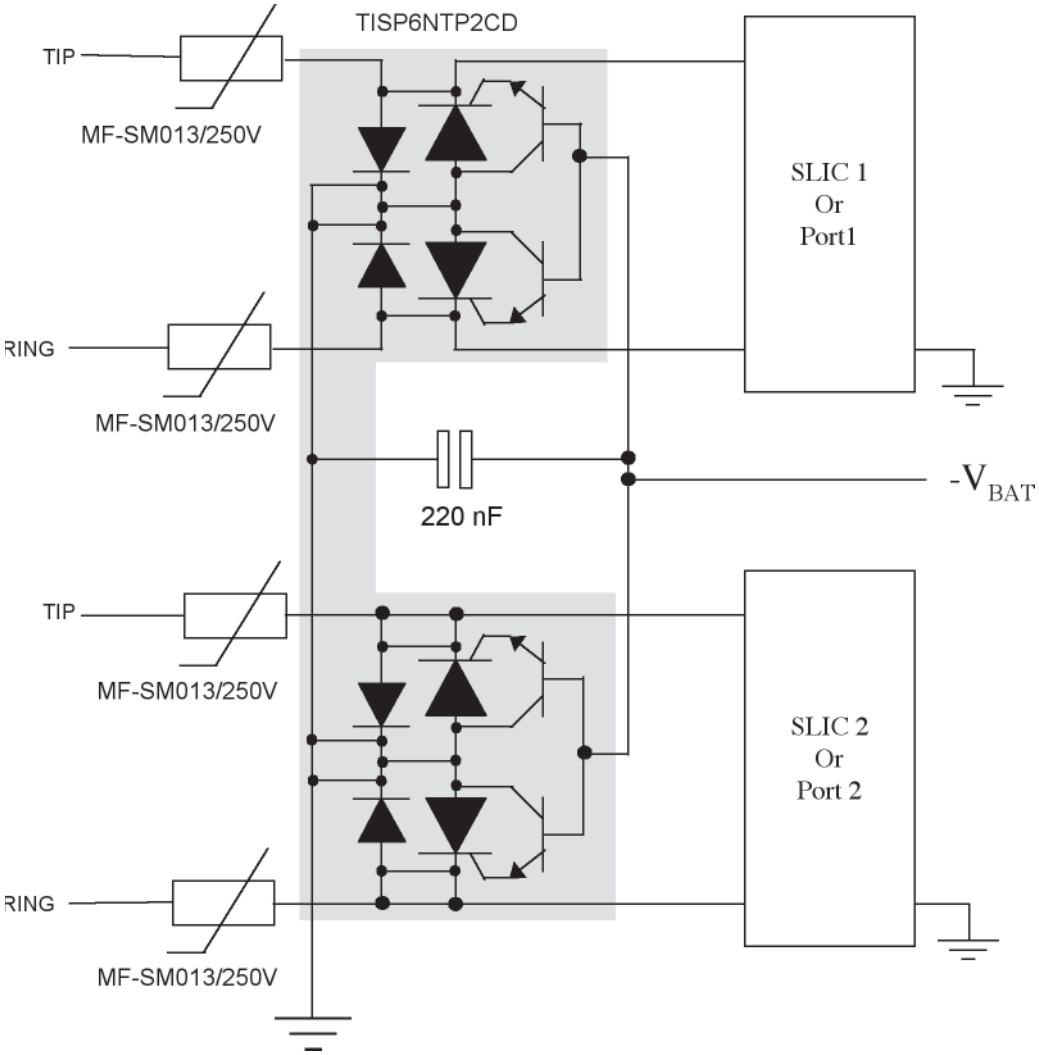



***Figure 12*** *– Dual port protector for intra-building*

## *ITU-T recommendations*

The TISP61089BD for single port applications and the TISP6NTP2CD for dual port applications can be considered for ITU-T applications. The TISP61089BD is rated for 40 A, 5/310 µs for a junction temperature ($T_J$) of –40 °C to +85 °C where the TISP6NTP2CD is also rated at 40 A, but for a $T_J$ of 0 °C to +70 °C. If the TISP6NTP2CD is required to operate in ambient temperatures of -40 °C to +85 °C, the current rating should be derated to 25 A for 5/310 µs impulse.

## ITU-T basic recommendations

The impulse requirement for K.20 is 25 A, 5/310 µs and therefore the TISP61089BD or TISP6NTP2CD can be used without any additional resistance. K.21 and K.45 have a current requirement of 37.5 A where both TISP6 series can also be considered. A series resistor of at least 7 Ω will help ensure impulse coordination with the primary protector under the 4 kV test. The overcurrent protector should be rated for 230 V rms to pass the basic AC power cross tests where the Bourns® Multifuse® SM013/250-B or MF-RX018/250 device can be used. Integrated voice data (IVD) solutions are sensitive to additional series resistance where the MF-RX018/250 with its maximum resistance of 2 Ω can be considered as shown in Figure 13. However, the PTC resistance will not ensure coordination with the primary protector as discussed on page 36, coordination requirements.

## ITU-T enhanced recommendations

The enhanced impulse increases the K.20 recommendation to 37.5 A and the coordination impulse voltage (with the GDT in place) is increased to 6 kV. The enhanced AC power contact tests range from 450 V rms to 1500 V rms between 0.18 s to 2 s. The test time can be calculated by using the formula on page 41, AC power line cross. The overcurrent protector will need to support the test voltage until enough voltage has been developed across the overcurrent protector to operate the GDT primary protector. 600 V polymer PTC components such as the MF-R015/600 may be required to help ensure suitable operation.

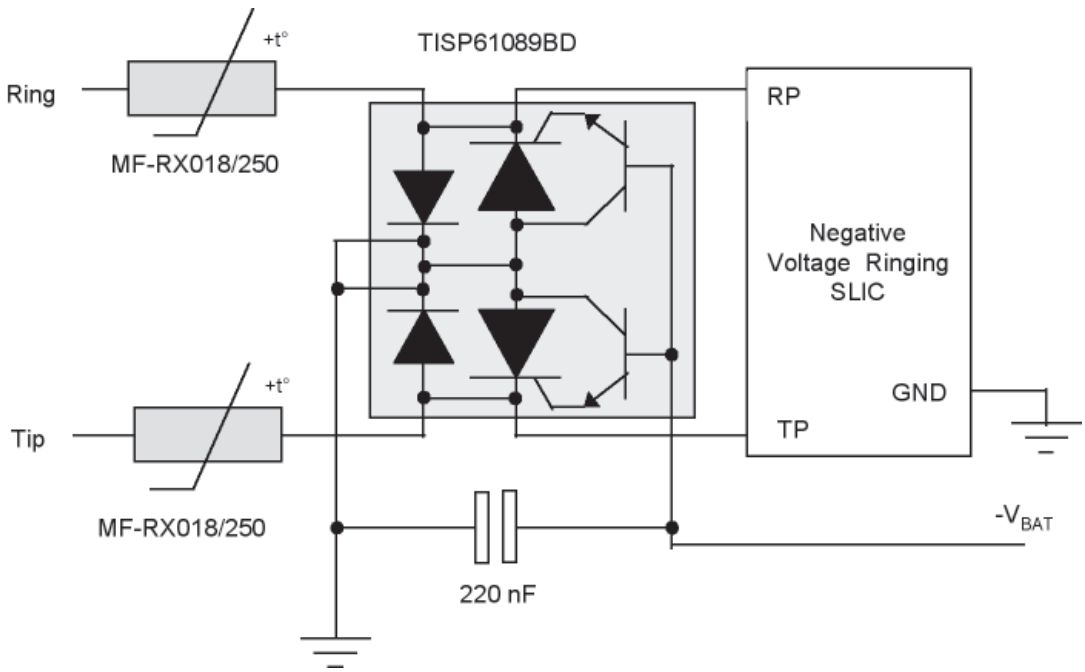



***Figure 13*** *– ITU-T basic recommendation*

***Note:*** *The MF-RX018/250 will not ensure primary coordination for basic test levels. To achieve this, a higher resistance value of 6 Ω for the PTC is required. The design engineer must ensure the PTC thermistor can support the AC and impulse requirements.*

# Application solutions for dual battery supplies

Dual voltage ringing SLICs require two thyristor protectors to reference to the positive and negative ringing battery voltage. The same design principles are used with the dual voltage protection SLICs as with the negative only protection solutions. The TISP8200MD gate reference is tied to the negative ring battery voltage and the TISP8201MD gate reference is connected to the positive ring voltage supply. Integrated architectures such as the TISP9110LDM have the same thyristor and buffer transistor topology to identify power supply connection.

### *Telcordia GR-1089-CORE, Issue 3 inter-building requirements*

GR-1089-CORE, Issue 2 would require a thyristor to meet 45 A to pass first level impulse requirements with a minimum 12.5 Ω resistor. This allowed the TISP8200MD and TISP8201MD dual voltage gated thyristors to be used. Protection coordination (Telcordia Technologies Generic Requirements, GR-1089-CORE, Issue 3, October 2002, section 4.6.7.1 protection coordination, page 4-15) is a new test for GR-1089-CORE for Issue 3 that can increase the 10/1000 µs impulse requirement of the circuit protection solution. Please see Appendix A, page 36, protection coordination for more information on coordination requirements for inter-building. The 4A12P-1AH-12R5 12.5 Ω module is designed to help ensure Issue 3 compliance with a GDT specified as the primary protector. The TISP8210MD and TISP8211MD are 60 A 10/1000 µs rated to help ensure conformance under the coordination test. The solution is shown in Figure 14.

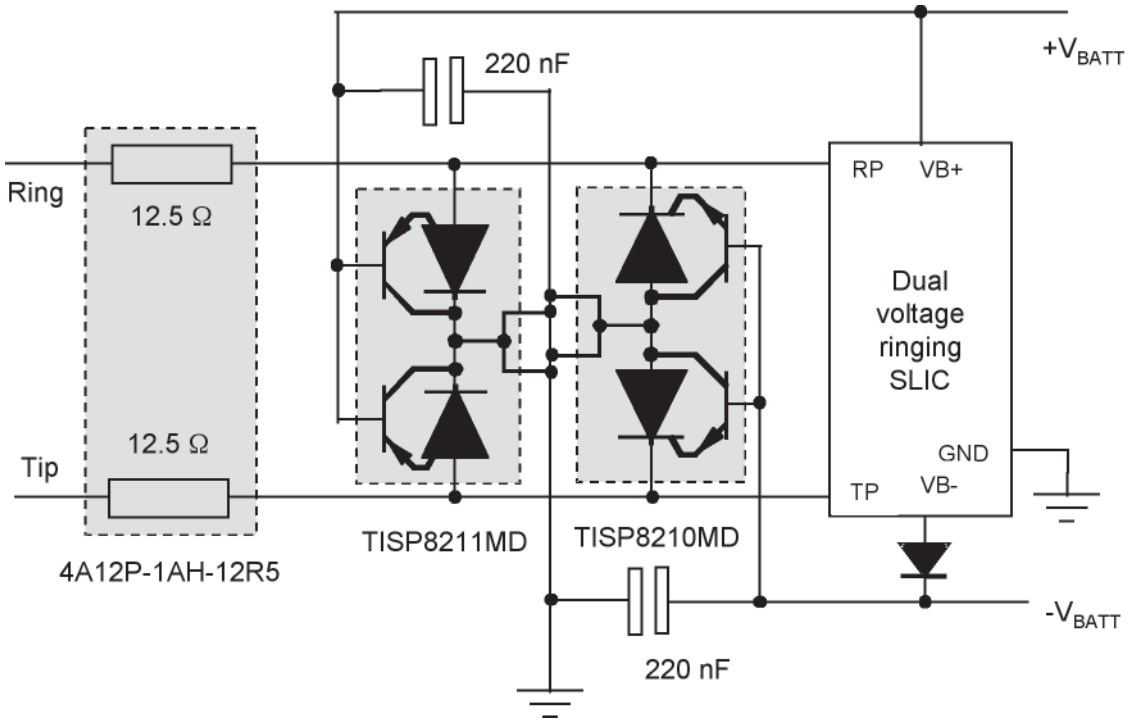



***Figure 14*** *– Dual voltage protection for inter-building requirements*

***Note:*** *At the time of writing this application note, a 100 A 10/1000 µs rated thyristor had not been released to allow the 1.25 A B1250T fuse to be used as the overcurrent protector. Please consult the factory for possible options.*

## *USA intra-building recommendations*

Customer premises equipment communication ports that do not leave the building do not have any circuit protection regulations. However, manufacturers recognize that equipment still needs to be protected to reduce field failure returns. Using just the TISP overvoltage protector increases the system withstand to impulse condition or engineers can consider the Telcordia GR-1089-CORE intra-building requirements.

This requirement is for internal (within the building) communication ports within the central office and is a good indication of electrical disturbances that can occur inside the building. GR-1089-CORE intra-building is covered in more detail in Appendix A, page 35, intra-building requirements.

GR-1089-CORE intra-building has a 100 A 2/10 µs test where the equipment must work after the test. The TISP9110LDM has a 2/10 µs capability of 100 A that helps ensure intra-building impulse requirements are achieved without the need of additional series resistance.

To meet the intra-building AC power contact test, the TISP9110LDM can be used with the Bourns® B0500T Telefuse™ Telecom fuse or the Bourns® Multifuse® MF-SM013/250 Polymer PTC thermistor where a typical circuit protection solution is shown in Figure 15. The TISP820xMD gated thyristors can be used if a higher protection solution is desired as these are 210 A 2/10 µs impulse rated.

***Note:*** *The 1.25 A B1250T single blow fuse is unsuitable to be used with either the TISP820xMD, TISP821xMD or TISP9110LDM. The B0500T fuse can be considered if a fuse is desirable.*

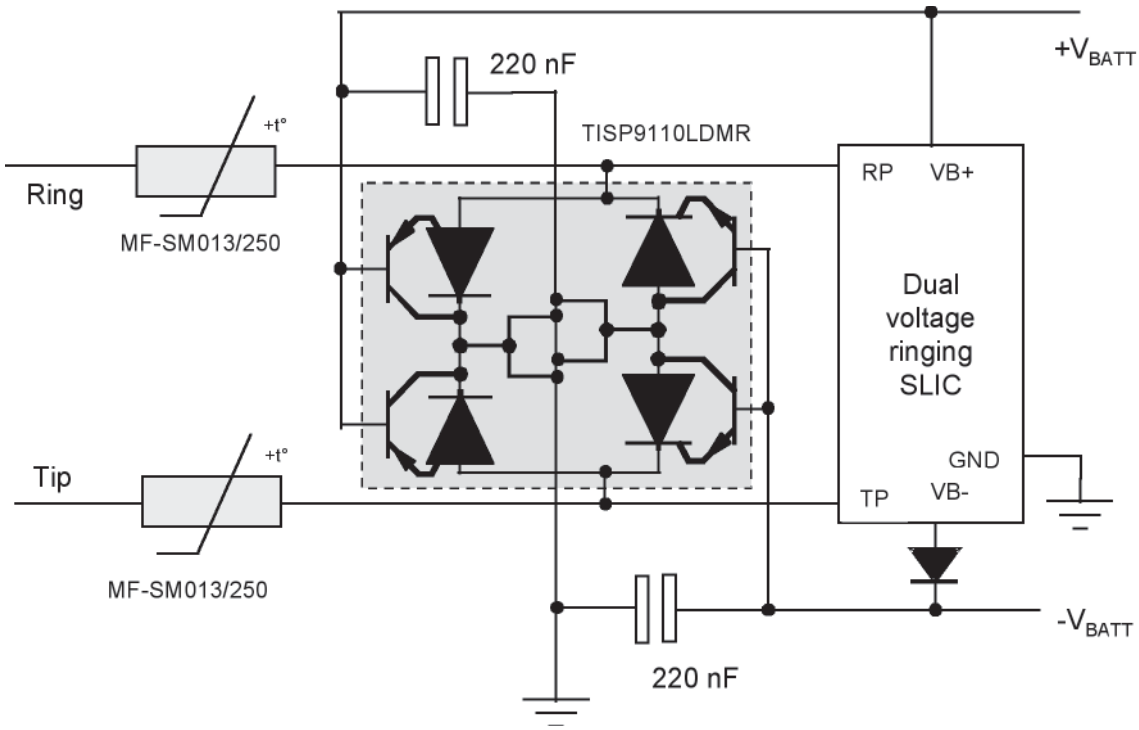



***Figure 15*** *– Intra-building protection solution*

### *ITU-T recommendations*

The TISP9110LDM is rated for 45 A 5/310 µs and therefore can support the basic and enhanced recommendations specified in K.20, K.21 and K.45. A series resistor of at least 7 Ω using the MF-SM013/250 with the TISP9110LDM will help ensure impulse coordination. The MF-SM013/250 is rated for 250 V rms to pass the basic AC power contact test. If coordination is not required and low series resistance is desirable, the MF-RX018/250 with its maximum resistance of 2 Ω can be considered as shown in Figure 16.

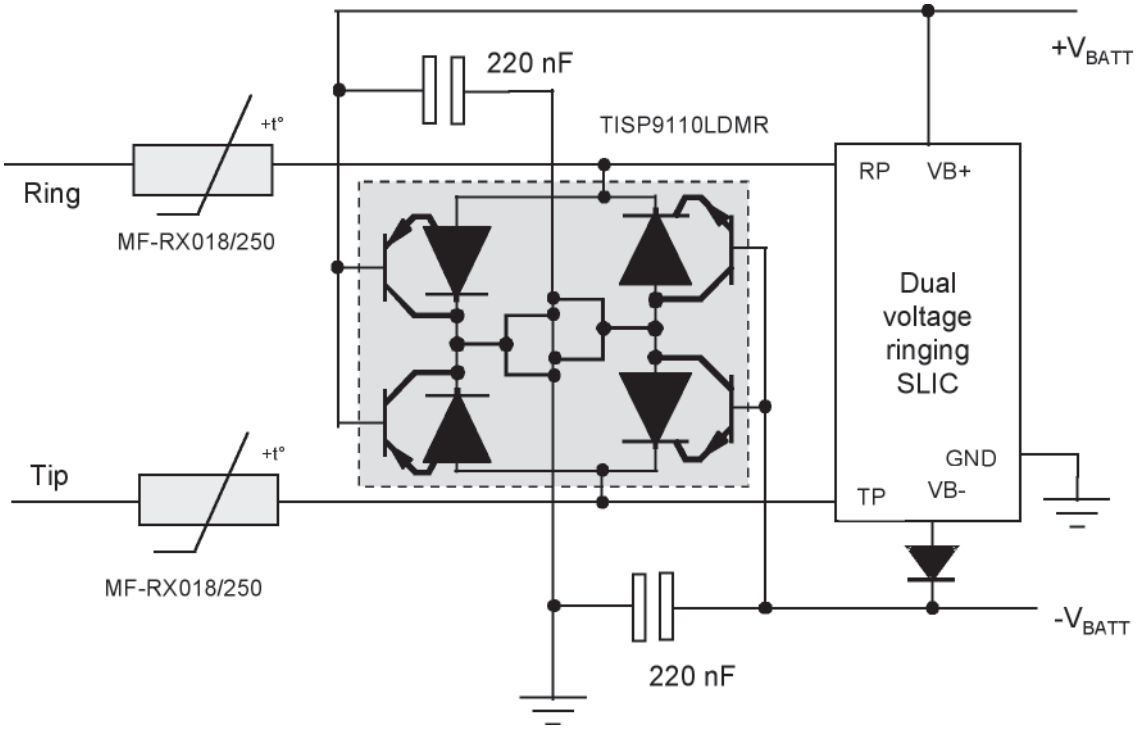



***Figure 16*** *– ITU-T basic recommendations protection solution*

## Enhanced AC test levels

The enhanced AC power contact tests range from 450 V rms to 1500 V rms between 0.18 s to 2 s. The test time can be calculated by using the formula highlighted on page 41, AC power line cross. The overcurrent protector will need to support the test voltage until enough voltage has been developed across it to operate the GDT primary protector. A 400 V or higher PTC component may be required to help ensure suitable operation. Bourns has 600 V rms PTC products such as the MF-R015/600-B-2 to be considered with the TISP820xMD or TISP821xMD thyristors.

The higher impulse TISP820xMD or TISP821xMD series will allow lower resistance values to be used where a minimum of 9 Ω can be considered. The minimum resistance for the TISP9110LDM is 35 Ω to meet ITU-T enhanced recommendations where a suitably rated ceramic PTC thermistor is recommended.

# Appendix A - Telecom standards

The country's standards or recommendations govern what protection is required for the equipment. Central office and remote access equipment in the USA need to conform to Telcordia GR-1089-CORE. Telcordia GR-1089-CORE intra-building requirements apply to central office ports that do not leave the building. Customer premises equipment (CPE) in the USA is required to meet TIA-968-A for lightning and UL 60950 (UL 1950) for AC power line cross that interface to external communication lines. CPE SLIC ports do not normally interface to the external TELCO lines and therefore are not covered in this document. CPE equipment ports that do not leave the building do not currently need to meet any impulse and AC tests, but protection is desirable to increase the robustness of the equipment and limit field returns. Reference to the Telcordia GR-1089-CORE intra-building requirements provides an indication of what level of protection should be considered.

Most other countries have adopted the ITU-T (International Telecommunications Union) recommendations. ITU-T is a recommendation and therefore countries can modify this document to suit their own requirements. The ITU-T recommendations break out into a series of documents where K.20 covers central office, K.45 for remote access equipment and K.21 for CPE. The ITU-T test method is provided in a separate document and covered in K.44. The ITU-T recommendations went through a major iteration in year 2000 to include a higher (enhanced) test level for locations that have severe lightning storms such as Japan and South Africa. The other significant addition is providing a primary and secondary protection impulse coordination test. Figure 17 indicates where the telecom standards are referenced in the communication highway.

This appendix will discuss the key areas of the standards and provide background material for selecting suitable overvoltage and overcurrent solutions.

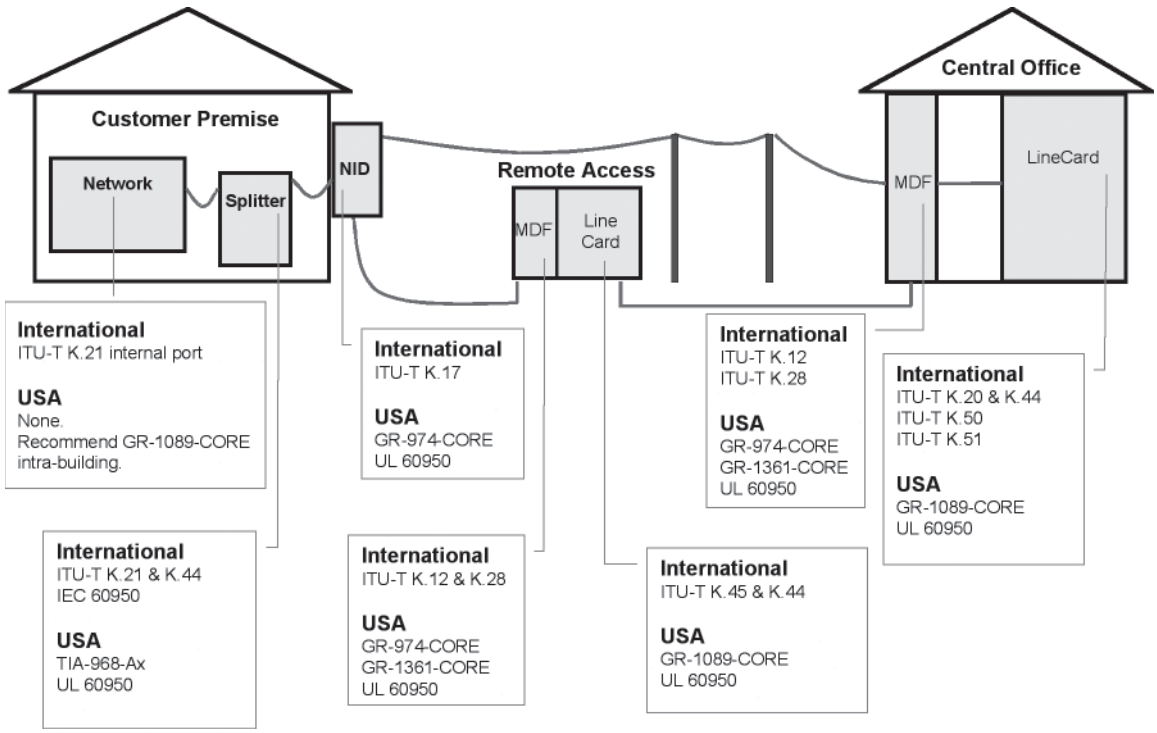



***Figure 17** – Overview of telecom standards*

## *USA Telcordia GR-1089-CORE (Issue 3) requirements*

The GR-1089-CORE standard (section 4) encompasses lightning and AC power fault test requirements for system protection. The GR-1089-CORE standards provide first-level tests where the equipment must function after the tests. Second-level tests allow the equipment to fail, but only in a safe mode and one that is not harmful to the network. Unbleached cotton cloth also known as "cheesecloth" is used as a fire or ejection hazard indicator where sufficient damage to destroy the structural integrity of the cloth will be classified as a failure.

Two-wire interfaces require metallic where $T_{LINE}$ and $R_{LINE}$ are connected to the test generator and longitudinal ($T_{LINE}$ & $R_{LINE}$ to GND) tests to be conducted on the equipment.

## First and second level surge

Table 3 shows the five first-level tests listed in Table 4-2 of GR-1089-CORE section 4.6.7. Tests three and four are normally performed on the equipment for approvals. Tests one and two can also replace test three if so required by the equipment manufacturer. The 10/1000 µs is a high-energy pulse where multiple pulses could cause a progressive temperature rise resulting in overcurrent protection device failure. Therefore, GR-1089-CORE specifies in section 4.6.1 that sufficient time may be allowed between surges to permit components to cool to ambient temperatures. A minimum test time of 40 seconds is used which is dictated by the impulse generator charge time. Test five is to be performed on twelve or less $T_{LINE}$ - $R_{LINE}$ pairs simultaneously and is used to test systems where telecommunication ports could share the same circuit protection solution. If the individual port protection meets tests three and four, then test five only confirms the current handling capability of common paths (600 A max).

| Test | Wave shape (t1/t2 µs) | Open circuit voltage | Short circuit current | Repetitions each polarity |
|---|---|---|---|---|
| **First-Level Surge** | | | | |
| 1 | 10/1000 | 600 V | 100 A | 25 |
| 2 | 10/360 | 1000 V | 100 A | 25 |
| 3 | 10/1000 | 1000 V | 100 A | 25 |
| 4 | 2/10 | 2500 V | 500 A | 10 |
| 5 | 10/360 | 1000 V | 25 A | 5 |
| **Second-Level Surge** | | | | |
| 1 | 2/10 | 5000 V | 500 A | 1 |

***Table 3** – Telcordia GR-1089-CORE impulse*

## First and second level AC power fault

Power companies and the telecommunications service providers often share the same trunking to the facility or building and therefore there is a possibility that the telecommunication lines can come into contact with the electrical source. The magnetic field produced by the currents in the power line under fault conditions can also be induced through electromagnetic coupling with the communication lines. The characteristic of the fault condition will govern if the primary line protector such as the carbon block or gas discharge tube (GDT) activates or long, low voltage time fault conditions occur.

The first and second level AC power fault tests are conducted under a 50 or 60 Hz sinusoidal waveform and are tested in metallic and longitudinal configurations. The 1000 V rms recommendations in issue 2 have been included as requirements in Issue 3. If the primary protector has not been defined in the system, the secondary protection circuit will need to support the full 1 kV rms test. This has been added to simulate the end of life carbon block characteristic in the field. The test number also highlights the number of applications for each test.

| First-Level AC power fault | | | |
|---|---|---|---|
| **Test #** | **Open Circuit Voltage (V rms)** | **Short Circuit Current (A)** | **Duration (s)** |
| 1 x 1 | 50 | 0.33 | 900 |
| 2 x 1 | 100 | 0.17 | 900 |
| 3 x 60 | 600 | 1 | 1 |
| 4 x 60 | 1000 | 1 | 1 + *Pri |
| 6 x 1 | 600 | 0.5 | 30 |
| 7 x 5 | 440 | 2.2 | 2 |
| 8 x 5 | 600 | 3 | 1.1 |
| 9 x 5 | 1000 | 5 | 0.4 +*Pri |

** Pri = Primary protector is in place during the test*

| Second-Level AC power fault | | | |
|---|---|---|---|
| **Test** | **Open Circuit Voltage (V rms)** | **Short Circuit Current (A)** | **Duration (s)** |
| 1 | 277 | 25 | 900 |
| 2 | 600 | 60 | 5 |
| 3 | 600 | 7 | 5 |
| 4 | 600 | 2.2 | 900 |

***Table 4*** *–Telcordia GR-1089-CORE AC power contact*

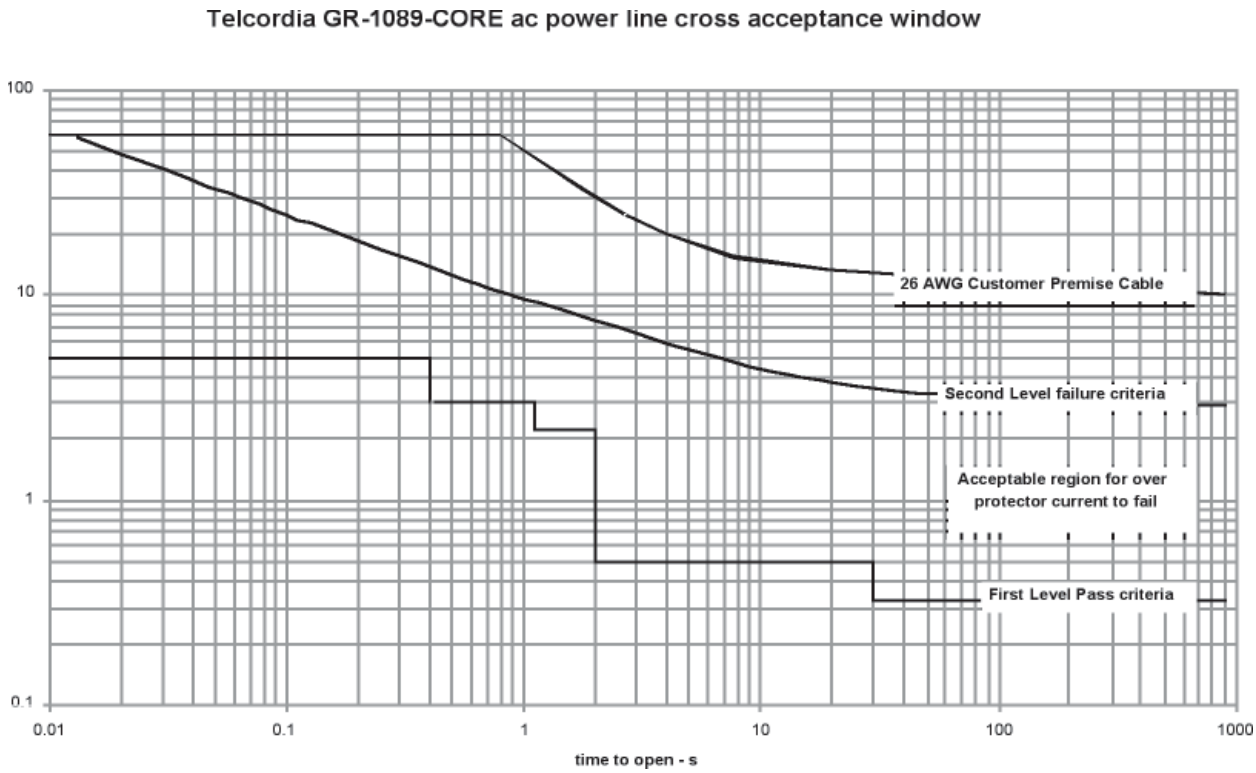
## Current-limiting protector tests

The current-limiting tests are conducted with 600 V rms, with a range of short circuit currents of 15-minute durations under metallic and longitudinal configurations. An external current limiter indicator that is time/current dependent is used to ensure conformance, but time/current measurements can be also taken. A MQD 1-6/10A or MDL 2.0A fuse manufactured by Bussman or their equivalent has been recommended as a suitable external indicator. This places the emphasis on the equipment to ensure this indicator fuse is not damaged during test. Designing the system so that it will not fail is not a possibility without providing current limiting below the fuse indicator characteristic. Cheesecloth is also applied to the equipment as the fire hazard and fragmentation indicator.

All the tests are performed on the equipment where test one and two do not require the external current limit indicator to be present. The equipment passes the other tests if the equipment interrupts the line current to less than 50 mA and the external current limiter indicator is not open circuit. If the external current limiter indicator is open circuit, the equipment will require external current limiting protectors. The first level pass criteria shows the boundary where the overcurrent protector must not interrupt and the second level failure criteria boundary where the protector must operate to allow conformance. The area between these two boundaries provides a window where the overcurrent protector must operate during the tests as shown in Graph 10, page 35.

| Test | Short Circuit Current (A) | Open Circuit Voltage (V rms) | Duration (s) |
|---|---|---|---|
| 1 | 2.2 | 600 | 900 |
| 2 | 2.6 | | |
| 3 | 3 | | |
| 4 | 3.75 | | |
| 5 | 5 | | |
| 6 | 7 | | |
| 7 | 10 | | |
| 8 | 12.5 | | |
| 9 | 20 | | |
| 10 | 25 | | |
| 11 | 30 | | |

***Table 5*** *–Telcordia GR-1089-CORE current limiting*




***Graph 10*** *– GR-1089-CORE AC power line cross acceptance window*

For applications where the manufacturer specifies the complete installation of the equipment from the network interface to the equipment, the MDL 2.0A fuse wiring simulation is replaced with a 30 cm section of 26 AWG copper cable. This will allow a higher current limiter to be used in the equipment giving more impulse current capability for remote terminal environments that can have surge current stress levels exceeding 100 A, 10/1000 µs.

## Intra-building requirements

Intra-building specifications apply to communication lines that only stay within the building with no external connections. Lightning disturbance can enter the building through earth reference disturbance or electromagnetic coupling of lightning rods for example. Communication lines to service off-site equipment will need to conform to Telcordia GR-1089-CORE in its entirety.

Two wire communications lines will need to be tested with metallic surges of a 2/10 µs waveform with an open circuit voltage of ±800 V and short circuit current of 100 A. The equipment also needs to withstand a longitudinal test with a waveform of 2/10 µs and an open circuit voltage of ±1500 V with a short-circuit current of 100 A. The equipment needs to withstand a single impulse of each polarity without damage under these tests.

It is key to note that if the communication lines are shielded and terminated to ground at both ends, the impulse test does not need to be done.

Intra-building has an AC power contact test (GR-1089-CORE, Issue 3 section 4.6.17, second level intra-building AC power fault tests for network equipment to be located on the customer premises, page 4-37). The test is conducted with 120 V rms, 25 A for 900 seconds where the equipment can fail safely. An external wire simulator using a MDQ 1-6/10 A or MDL 2.0 fuse is used to help ensure the equipment port does not consume excessive currents that can damage the interconnect leads.

## Protection coordination

Protection coordination is a new objective for GR-1089-CORE Issue 3. The change to a requirement on January 1, 2006 has been postponed until issue 4 has been released. This coordination references GR-974-CORE TLPUs (Telecommunications Line Protector Units) for primary protection with secondary protection. The equipment communication lines will initially be tested at the specified primary voltage protector. If a primary protector is not defined or will be used with a carbon block primary, the test will start with an open circuit generator voltage of 1000 V and increase in steps of 200 V to a maximum of 2000 V or until one of the two following criteria is achieved:

*A. The communication lines are stressed to at least 1000 Vpeak ($V_P$) across the equipment terminals. For example, if the generator impedance is 10 Ω (1000 V/100 A) and the equipment has an overcurrent resistor of 50 Ω, the generator open circuit voltage will need to be set to 1200 V to achieve 1000 V across the terminals.*

*B. The peak current ($I_{PP}$) into the equipment terminals exceeds 100 A. This can be achieved by replacing $R_{SERIES}$ with a fuse such as the Bourns® B1250T Telefuse™ Telecom fuse. The generator open circuit voltage will be set to 1000 V to achieve 100 A into the equipment.*

The equipment fails the coordination requirement if neither A nor B is achieved with a maximum generator voltage of 2000 V or the equipment is damaged and does not operate as intended.

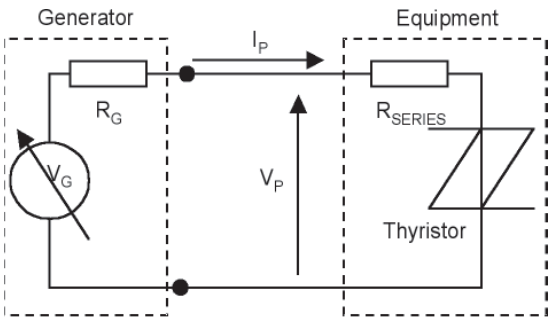



***Figure 18** – Coordination requirements*

If the primary protector is defined, the voltage limiting specification can be a maximum of either 400 V or solid-state primary or 600 V for GDT primary. This primary protector will denote the initial generator start voltage and the $V_P$ voltage to meet criteria A or B. The coordination test will be conducted with a 10/1000 µs waveform where the test requires ten repetitions per polarity. The communication lines will also be tested to metallic and longitudinal procedures to ensure conformance.

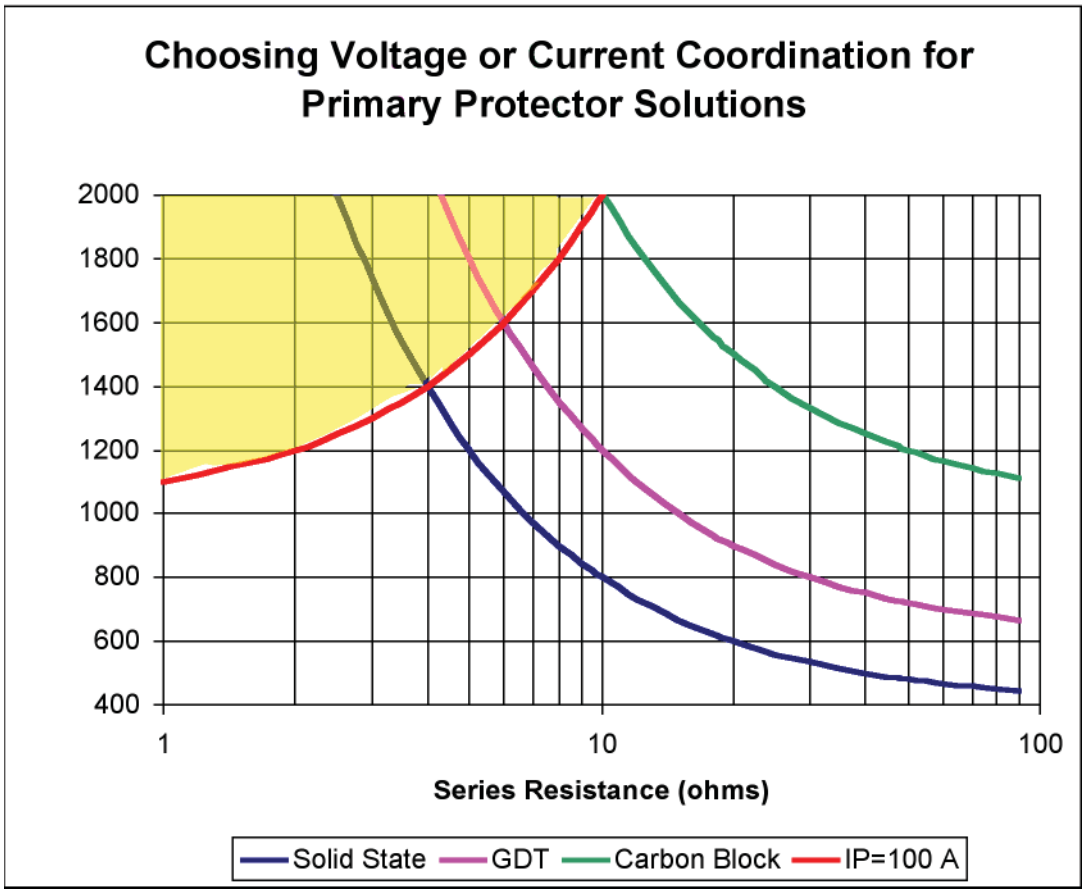
There is a trade off between the generator voltage and the series resistance selected. For example, if the $R_{SERIES}$ value is 10 Ω, the generator voltage will need to be adjusted to 2000 V to achieve coordination with a carbon block but if $R_{SERIES}$ were 50 Ω the $V_{GEN}$ would be 1200 V. Increasing the series resistance will increase the power dissipation requirements of the module under first level AC power contact tests that is covered on page 20, power dissipation in the LFR. This new test will penalize high series resistance (15-50 Ω) that benefits actual true coordination where the secondary resets after the disturbance. The first level 10/1000 µs impulse will generate 500 V with a series resistance of 10 Ω and the thyristor could be derated to 50 A. However, the new coordination requirements will provide a stress voltage of 1000 V across the 10 Ω series resistor where the thyristor will need to support 100 A which increases the withstand capability two fold from the old issue 2 requirements.

Defining the primary protector can also reduce the stress of the circuit protection components. If a GDT such as the Bourns® 2026-35-C2F or 2410-31-G-MSP 5-pin module solution is specified as the primary protector, the maximum open circuit generator voltage will be 1200 V to achieve a $V_P$ of 600 V. This will allow an 80 A 10/1000 µs rated thyristor to be considered in the application and the rating of the 10 Ω to be closer to the first level impulse test requirement.

Bourns® Telcordia GR-1089-CORE Issue 3 modules require a GDT or solid-state primary protector to be specified with the equipment.

Graph 11 highlights where the series resistance ($R_{SERIES}$) will dictate a current or voltage coordinated application across the three primary protector options. The three options are carbon block or none specified, GDT or a solid-state (semiconductor) primary protector. For applications requiring voltage coordination, the additional series resistance, $R_{SERIES}$ must be outside the shaded area (right of IP curve) on Graph 11. For example, a line card defined with a GDT primary protector will be voltage-coordinated with a series resistance of greater than 6 Ω and current-coordinated with less than 6 Ω. The maximum power transfer will occur at the crossover point of 6 Ω, which will be the highest stress factor for the series resistance. At 6 Ω, the series resistance will need to support an open circuit generator voltage of 1600 V and 100 A 10/1000 µs.

***Note:*** *The maximum power transfer points should be avoided if possible.*




***Graph 11*** *– Voltage or current coordination*

***Note:*** *Bourns® Telcordia GR-1089-CORE line feed resistor modules need to be defined with either a GDT or solid-state thyristor primary protector to pass the coordination requirements.*

### *ITU-T recommendations*

The ITU-T (International Telecommunication Union-Telecommunication Standardization Sector) K series protection recommendation is location based. K.20 covers central office equipment, K.45 for remote access equipment and K.21 for customer premises equipment (CPE). The test circuits for these documents are given in K.44. For 2003, the ITU-T K.15 (remote feed and line repeaters) and K.17 (power feed repeaters) are now addressed in K.45. K.22 (ISDN) is now included in K.21 and K.41 (Internal interfaces) are in K.20. ITU-T is a recommendation and therefore the individual countries can modify these recommendations and add tests specific to their telephone networks.

## External port impulse tests

A recent addition to ITU-T is to include enhanced test levels for countries that want increased impulse and AC power fault conditions. The new enhanced recommendations increase the open circuit impulse to 1.5 kV for K.20 central office applications. Field investigation also showed that customer premises equipment was more vulnerable to impulse than central office equipment and therefore the enhanced impulse is specified at 6 kV compared to basic 1.5 kV. Multiple port testing uses a 10/700 µs voltage surge where the generator output is resistively divided between the ports. The individual port stress will be generally lower for multiple-port testing than for single-port testing unless the inherent overvoltage protector is shared across several lines. This test will result in the highest ground-return currents in the application that needs to be considered in areas such as track thickness. Table 6 provides a summary of the external port impulse requirements.

The latest 2003 ITU-T recommendations include new tests to stress the external port to internal ports of the equipment. In 2002 ITU-T, the internal ports such as USB, ethernet connections on modems were left floating. Under the latest recommendation, the internal ports are coupled to the ground return of the generator. This will test the withstand capability between the external and internal ports when the primary protector is not used. All the untested ports are tested in their terminated or powered modes and then tested with them coupled down to ground.

## Single and multiple port 8/20 µs current testing

Year 2003 ITU-T tests 2.1.5 and 2.1.6 have been included to address applications that remove the need of an external primary protector by having the primary protection inside the equipment. The standard specifies 1 kA per wire where the additional external resistance is zero. As the additional output resistance is zero, the ideal test procedure is to use a generator with multiple outputs. This reduces the possibility of one line protector switching on first and all the test current going through the protector.

## Coordination requirements

Primary equipment protection coordination must now be verified during longitudinal and metallic (transverse) impulse testing as set out in K.44. If the equipment meets K.28 (solid-state primary), this coordination test can be omitted. The 2003 ITU-T recommendations have also included port to external port testing for K.21 and K.45 applications. The enhanced coordination recommendations for K.20 will be tested with 4 kV with an additional external resistance of 25 Ω for applications with less than 250 lines (125 ports). The additional series coordination resistance may need to be increased for applications. This is due to the impulse current path going through the tested port primary protector ground to another external port primary protector and returning to the generator through the external port coupling element. This will place the primary protectors in series so that a higher coordination voltage will need to be generated to operate the primary protection. The current path will be the same if the secondary protection to the equipment ground is used. When the GDT on the tested port operates, coordination is checked at the highest impulse level of 10/700 µs at 4 kV, 2 x 80 A (basic) or 6 kV, 2 x 120 A (enhanced) where the primary is verified to switch during the test. The equipment is tested five times in each polarity to ensure coordination.

| $V_{GEN}$ | Port-GND | Port-Port |
|---|---|---|
| 4 kV | 6.6 Ω | 6.9 Ω |
| 6 kV | 4.1 Ω | 4.2 Ω |
| 10 kV | 2.4 Ω | 2.4 Ω |

***Table 6** – Coordination resistance*

<table>
<tr><th rowspan="2">Port</th><th rowspan="2">Test</th><th rowspan="2">Lighting Test</th><th colspan="3">Basic test levels</th><th colspan="3">Enhanced test levels</th><th rowspan="2">No of tests</th><th rowspan="2">Primary protection</th></tr>
<tr><th>K.20</th><th>K.45</th><th>K.21</th><th>K.20</th><th>K.45</th><th>K.21</th></tr>
<tr><td rowspan="10"></td><td>2.1.1.a</td><td>10/700 µs longitudinal</td><td>1 kV R=15+25</td><td colspan="2" rowspan="3">1.5 kV</td><td colspan="2" rowspan="2">1.5 kV</td><td></td><td rowspan="10">5 at each polarity</td><td rowspan="3">No</td></tr>
<tr><td>2.1.1.b</td><td>10/700 µs transverse</td><td rowspan="2">1.5 kV,<br>Case insulation tested to 6 kV</td></tr>
<tr><td>2.1.1.c</td><td>10/700 µs port to external port</td><td>NA</td><td>Note</td><td></td></tr>
<tr><td>2.1.2.a</td><td>10/700 µs coordination longitudinal</td><td colspan="3" rowspan="2">4 kV</td><td colspan="2" rowspan="2">4 kV</td><td rowspan="3">6 kV</td><td rowspan="3">Yes special primary test protector</td></tr>
<tr><td>2.1.2.b</td><td>10/700 µs coordination transverse</td></tr>
<tr><td>2.1.2.c</td><td>10/700 µs coordination port to external port</td><td>NA</td><td></td><td></td><td>Note</td><td></td></tr>
<tr><td>2.1.5.a</td><td>8/20 µs longitudinal</td><td colspan="3">1 kA per wire</td><td colspan="3">5 kA per wire</td><td rowspan="2">No</td></tr>
<tr><td>2.1.5.b</td><td>8/20 µs port to external port</td><td>NA</td><td></td><td></td><td>Note</td><td></td><td></td></tr>
<tr><td rowspan="6"></td><td>2.1.3.a</td><td>10/700 µs inherrant longitudinal</td><td colspan="3">4 kV</td><td colspan="3">6 kV</td><td rowspan="2">No</td></tr>
<tr><td>2.1.3.b</td><td>10/700 µs port to external port</td><td>NA</td><td></td><td></td><td>Note</td><td></td><td></td></tr>
<tr><td>2.1.4.a</td><td>10/700 µs longitudinal</td><td colspan="3">4 kV</td><td colspan="3">6 kV</td><td rowspan="2">Yes agreed protector</td></tr>
<tr><td>2.1.4.b</td><td>10/700 µs port to external port</td><td>NA</td><td></td><td></td><td>Note</td><td></td><td></td></tr>
<tr><td>2.1.6.a</td><td>8/20 µs longitudinal</td><td colspan="3">(limited to maximum 6 kA)</td><td colspan="3">(limited to maximum 30 kA)</td><td rowspan="2">No</td></tr>
<tr><td>2.1.6.b</td><td>8/20 µs port to external port</td><td>NA</td><td></td><td></td><td>Note</td><td></td><td></td></tr>
<tr><td colspan="11">Note: Systems with greater than 250 Ports do not need to be tested. Systems with less than 250 ports will be tested to K.45 requirements.</td></tr>
</table>

***Table 7** – ITU-T impulse*

***Note:** ITU-T impulse table was sourced from Compliance Engineering article "The 2003 ITU-T Telecommunications Equipment Resistibility Recommendations".*

K.44 (Appendix 1 of the testing procedure) covers increased coordination open circuit test voltages up to 10 kV, 25 Ω with a 10/700 µs to address applications such as CPE equipment that could have poor primary protection. As the voltage coordination increases, the minimum coordination resistance reduces. This places the emphasis on the equipment coordinating at the basic 4 kV impulse test, but the coordination resistor meeting the higher stress levels induced with the 10 kV test.

## Internal port impulse tests

The 2003 ITU-T recommendations now includes internal port testing where telecommunication lines do not leave the building or interface to outside plant equipment and is the same as Telcordia GR-1089-CORE intra-building requirements. A summary of the impulse test is highlighted in Table 7. ITU-T internal port testing only tests with 8/20 µs impulse conditions and does not include AC power contact recommendations like GR-1089-CORE. Single port applications are tested with an additional external resistance of 10 Ω. For a two-port application, a single port will be tested, with the second port powered and terminated. The TIP and RING lines will be tested with its own external 10 Ω series resistor for single output generators to ensure the current is shared between both conductors. The additional external 10 Ω series resistor changes the short circuit current to a 3.3/30 µs as the fictive resistance of the generator is now 12 Ω. This provides a harsher requirement than the original 8/20 µs test.

Multiple port applications with unshielded lines are tested with the other ports powered, terminated or left open. The ports are tested with an 8/20 µs (open circuit voltage waveform is 1.2/50 µs) waveform with an additional 10 Ω of external resistance that also changes the current waveform to 3.3/30 µs.

| Port | Test | Lighting Test | Basic test levels | | | Enhanced test levels | | | No of tests | Primary protection |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | K.20 | K.45 | K.21 | K.20 | K.45 | K.21 | | |
| | 7.1 | 8/20 µs unshielded cable longitudinal | 500 V R=2+10 | NA | 1 kV R=2+10 | 1 kV R=2+10 | NA | 1.5 kV | 5 at each polarity | No |
| | 7.2 | 8/20 µs shielded cable longitudinal | 500 V | NA | 1 kV | 1 kV | NA | 1.5 kV | | No |

***Table 8*** *– ITU-T internal or intra-building impulse*

***Note:*** *ITU-T internal or intra-building impulse table was sourced from Compliance Engineering article "The 2003 ITU-T Telecommunications Equipment Resistibility Recommendations".*

Ports with shielded cabling are tested in the multiple port configuration where the individual lines and shield are connected together directly to 8/20 µs without any additional series resistance. The equipment is tested with a 20 m length of shielded cable where the cable resistance is expected to ensure current sharing between the ports. Internal port tests do not apply to K.45 (remote access), that will rely on external port testing procedure.

## AC power line cross

The ITU-T recommendation specifies eight source-resistance values ranging from 10 to 1000 Ω to be tested with a 50-60 Hz 230 V rms generator. The test range can be narrowed if the worse case stress conditions of the equipment are known. Enhanced power contact testing uses the same resistance and voltage levels, but the equipment is also required to meet criterion A (equipment must not fail in operation) for the resistance ranges of between 160 to 600 Ω.

The inherent induction test is achieved with a 600 V rms, 0.2 s, 600 Ω applied to the equipment where the equipment must still operate as intended. Basic coordination testing increases the test time to 1 s, 600 Ω applied to the different configurations with the primary protector in place. Enhanced coordination testing is done with a 200 Ω generator source with various voltage and time values set between 1500 V rms for 0.18 s and 450 V rms for 2 s. The time versus test voltage can be calculated by using the formula -

$$t = \frac{400{,}000}{V^2} \text{ seconds}$$

K.44 highlights testing at 450 V & 1500 V and then at least two intermediate levels between the two should be sufficient if there are no transitions specified.

ITU-T does not distinguish between single and multiple ports under AC fault conditions and therefore each port is considered a single port solution. The table below shows the AC tests for single port applications.

<table>
<tr><th rowspan="2">Test No</th><th rowspan="2">Power test description</th><th colspan="3">Basic test levels</th><th colspan="3">Enhanced test levels</th><th rowspan="2">No of tests</th><th rowspan="2">Primary protection</th><th rowspan="2">Acceptance criteria</th></tr>
<tr><th>K.20</th><th>K.45</th><th>K.21</th><th>K.20</th><th>K.45</th><th>K.21</th></tr>
<tr><td>2.2.1.a</td><td>Induction inherent longitudinal</td><td colspan="6" rowspan="2">$I^2t$ = 0.2 $A^2s$<br>600 V rms max<br><br>t=0.2 s</td><td rowspan="3">5</td><td rowspan="3">No</td><td rowspan="6">A</td></tr>
<tr><td>2.2.1.b</td><td>Induction inherent transverse</td></tr>
<tr><td>2.2.1.c</td><td>Induction port to external port</td><td>NA</td><td></td><td></td><td>Note</td><td></td><td></td></tr>
<tr><td>2.2.2.a</td><td>Induction inherent coordinational longitudinal</td><td colspan="3" rowspan="2">$I^2t$ = 1 $A^2s$<br>600 V rms max<br><br>t=1 s</td><td colspan="3" rowspan="2">$I^2t$ = 10 $A^2s$<br>450 V rms to 1500 V<br><br>t=0.18 s to 2 s<br>$t=400k/V^2$</td><td rowspan="3">5 at each test level</td><td rowspan="3">Yes agreed primary or special primary test protector</td></tr>
<tr><td>2.2.2.b</td><td>Induction inherent coordination transverse</td></tr>
<tr><td>2.2.2.c</td><td>Induction coordination port to external port</td><td>NA</td><td></td><td></td><td>Note</td><td></td><td></td></tr>
<tr><td>2.3.1.a</td><td>Contact longitudinal</td><td colspan="3" rowspan="2">230 V rms,<br>R = 10, 20, 40, 80, 160,<br><br>t=900 s for each resistor value</td><td colspan="3" rowspan="2">230 V rms,<br>Criteria B for R = 10,<br><br>Criteria A for R = 160,<br><br>t=900 s for each resistor value</td><td rowspan="3">1 set</td><td rowspan="3">No</td><td rowspan="3">B</td></tr>
<tr><td>2.3.1.b</td><td>contact transverse</td></tr>
<tr><td>2.3.1.c</td><td>Contact port to external port</td><td>NA</td><td></td><td></td><td>Note</td><td></td><td></td></tr>
<tr><td colspan="11">Note: Systems with greater than 250 Ports do not need to be tested. Systems with less than 250 ports will be tested to K.54 requirements.</td></tr>
</table>

***Table 9*** *– ITU-T single port AC power cross*

***Note:*** *ITU-T single ports AC power cross table was sourced from Compliance Engineering article "The 2003 ITU-T Telecommunications Equipment Resistibility Recommendations".*

# Appendix B - Gated thyristor protection evolution

Fixed voltage thyristors have between 25-35 % voltage difference between the maximum working voltage, $V_{DRM}$ and the protection voltage $V_{(BO)}$. Gated thyristor solutions are referenced to the battery voltage of the SLIC. This allows the system to be protected at the system voltage to allow tighter protection (3 % or less). Gated thyristors also provide the lowest overstress condition to the SLIC during an overvoltage stress condition.

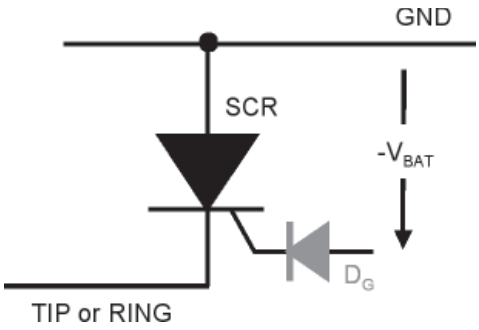



***Figure 19*** *– basic gated thyristor solution*

The gated protector was first implemented in the early 1980s by using a P-gate Silicon Controlled Rectifier (SCR) thyristor. The battery tracking feature was designed by referencing $-V_{BAT}$ to the SCR gate. The standard SCR would allow the TIP or RING of the telephone line to be protected to approximately -0.7 V from $-V_{BAT}$. The problem with the circuit was that the SCR would try to take the gate pin to ground along with the cathode connection when the SCR conducted to ground. Therefore, a diode $D_G$ as shown in Figure 19 was required to block the reverse gate current when the SCR was in the conduction mode. The inclusion of $D_G$ made the protection voltage of the circuit increase slightly to -1.4 V below $-V_{BAT}$.

The gate diode was replaced with a NPN buffer transistor to provide a current gain on the gate current. The gate trigger current significantly dropped from 100 mA to around 1 mA with the transistor current gain of 100. The negative battery supply could have difficulty in sourcing high gate currents for a period under long AC contact conditions. The low gate current of the buffered gate thyristor helps to ensure the $-V_{BAT}$ supply does not go unregulated by having too much current demand under fault conditions. Another disadvantage of the diode-gated thyristor is that a positive charge, Qg is reflected through the SCR cathode during switching. This has the effect of causing the negative battery supply voltage (dc/dc converter) to go more negative. If the system cannot support this extra charge, the regulator may stop regulating since it cannot sink current and the supply goes more negative. The increase in $-V_{BAT}$ could be enough to damage the SLIC. A common "tell-tale" sign are SLICs failing randomly under impulse tests although the port is not being tested. The buffer-gated thyristor almost eliminates the positive current effects with its transistor gain and helps to ensure the switch mode power supply stays sourcing current. Negative gated thyristors are commonly used on negative voltage ringing SLICs that deploy unbalanced or battery-backed ringing topologies. The buffer transistors, thyristors and diodes are integrated into a single package as shown in Figure 20 to provide a single port protection solution.

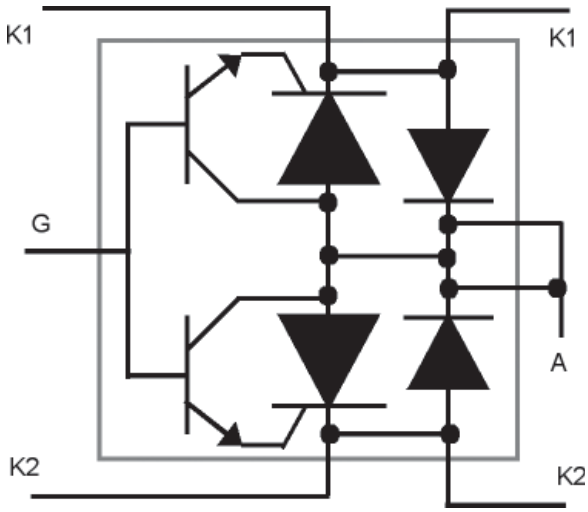



***Figure 20*** *– TISP61089 schematic*

## Dual voltage ringing SLICs

Dual voltage ringing SLICs require a positive buffered gated thyristor protection solution that tracks the $+V_{BAT}$ supply. An N-channel SCR is used with a PNP buffer transistor as shown in Figure 21 to provide the positive gate reference. The SCR will operate with the anode approximately 1.4 V above the PNP positive reference voltage. The repetitive peak reverse voltage ($V_{RRM}$) withstand of the positive and negative SCRs must be above the maximum battery voltages. The same design principles are used with the dual voltage battery tracking devices as with the single supply options.

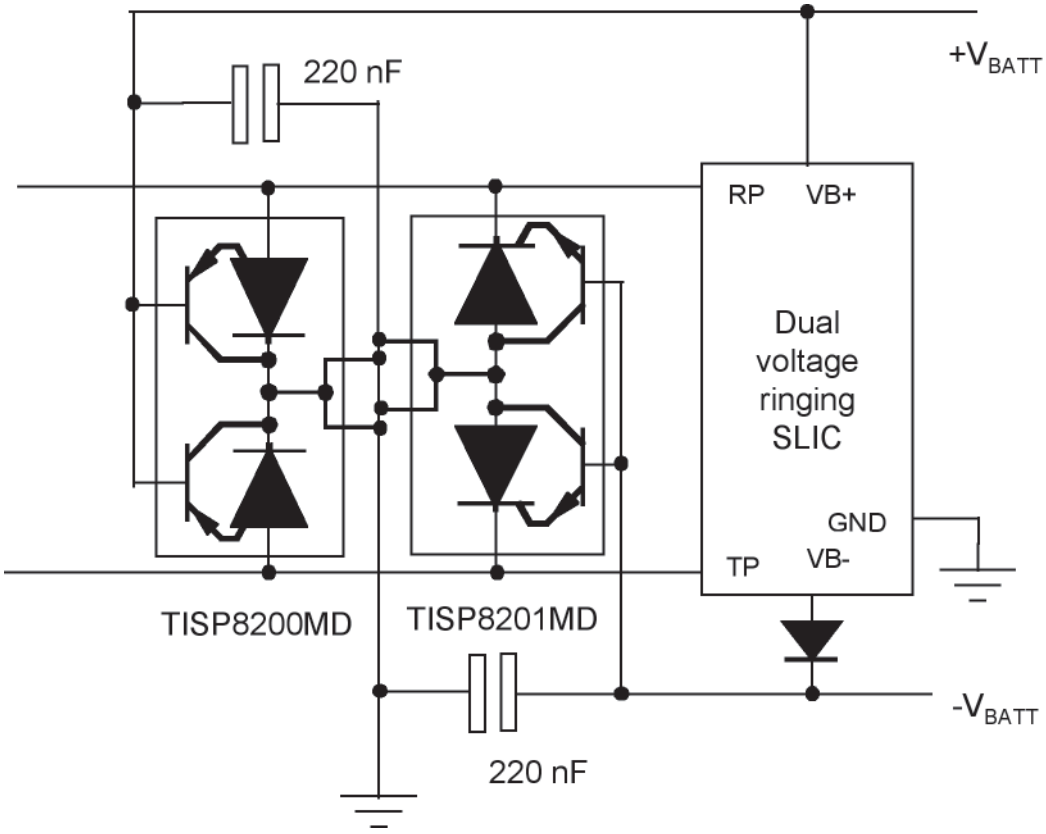



***Figure 21*** *– Dual voltage ringing SLIC protection*

# References

Telcordia Technologies Generic Requirements, GR-1089-CORE, Issue 3, October 2002, "Electromagnetic Compatibility and Electrical Safety – Generic Criteria for Network Telecommunications Equipment".

Mick J Maytum, 2002, "The New ITU-T Telecommunication Equipment Resistibility Recommendations" Compliance Engineering article.

Mick J Maytum, 2003, "The 2003 ITU-T Telecommunication Equipment Resistibility Recommendations" Compliance Engineering article.

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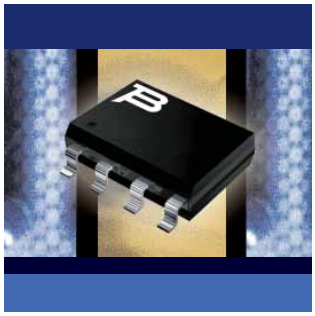

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