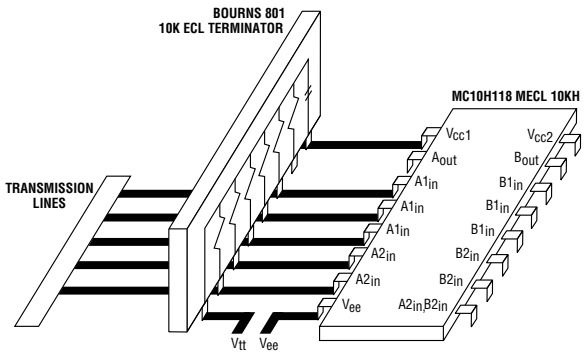
For complete product specifications, download Bourns' 800 Series data sheet.

Bourns Emitter Coupled Logic Terminator 800 Series

Typical Application

A typical application using a Bourns 801 RC Network in conjunction with a 10K ECL design is shown below. Vee is typically connected to -5.2 volts (10K ECL) or -4.5 volts (100K ECL). V_{cc} is typically connected to GND. V_{tt} is typically connected to -2.0 volts. The 801 network shown below can terminate up to 6 transmission lines and provides a 0.01 µF capacitor to reduce cross talk and feedthrough effects.



Transmission Line Considerations

In high speed circuit applications, the signal propagation delay (T_{pd}) and characteristic impedance (z_o), along a printed circuit board line must be taken into consideration. In general, if the two-way delay along the line is greater than the rise or fall time of the signal, then controlled impedance techniques (i.e., termination) must be utilized to prevent undesirable ringing or over- and undershoots. The delay and impedance can be calculated by knowing the intrinsic inductance (L_o) and capacitance (C_o) of the line:

$$T_{pd} = \sqrt{L_o C_o}$$

$$Z_o = \sqrt{L_o / C_o}$$

The actual, effective delay and impedance due to loading from stubs or additional devices off the line will be:

$$T_{pd}' = T_{pd}\sqrt{1 + C_d/C_o}$$

$$Z_o' = \sqrt{\frac{Z_o}{1 + (C_d/C_o)}}$$

Where C_o = intrinsic capacitance of the line
C_d = capacitance due to loading and stubs off the line
T_{pd} = basic propagation delay of the line
Z_o ....= basic impedance of the line

To formulate a guideline for when line termination is necessary, take the ratio of the rise time or fall time and the two-way delay along the line. The maximum length for unterminated lines will result as follows:

$$L_{max} = \frac{T_r}{2T_{pd}'}$$

Where T_r = rise or fall time
T_{pd} = propagation delay per unit length

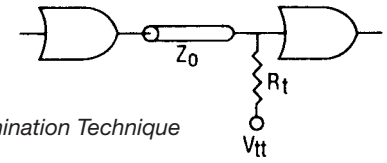
The above equation implies that the faster the edge rate or the higher the loading on the line (i.e., higher fanout), the more likely that termination will be necessary for a given line length.

Parallel Termination

For maximum circuit performance or distributed loads, parallel termination is the most appropriate technique. A parallel terminated line uses a resistor connected to -2 volts (ECL application) at the receiving end. The resistor value matches the characteristic impedance of the line (Z_o), thereby producing zero reflection at the receiver. In addition, the terminating resistor also provides output pull down, so a separate pull down resistor at the driving end is unnecessary.

Bourns Emitter Coupled Logic Terminator 800 Series

Bourns 801, 802, and 804 conformal coated SIP resistor capacitor networks are designed to terminate 6 transmission lines using the parallel termination technique. A 0.01 µF capacitor(s) is provided in each network to help maintain a solid Vtt level within the package, mitigating any potential cross talk or feedthrough effects. The 804 circuit also contains a 0.1 µF capacitor for bypassing the V_{ee} supply.



Parallel Termination Technique

Thevenin Equivalent Parallel Termination

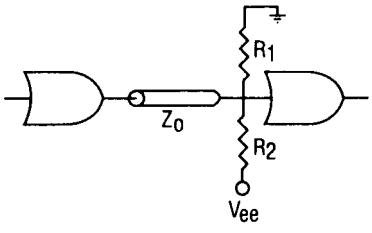
Parallel termination in ECL applications uses -2.0 volts as the terminating voltage. This represents a disadvantage since a separate V_{tt} power supply must be available (V_{ee} = -5.2 volts, V_{tt} = -2.0 volts). For systems in which a separate -2.0 volt supply is not available, the use of a Thevenin equivalent arrangement, although resulting in higher power consumption, provides a convenient solution.

Bourns 803 and 805 conformal coated SIP resistor capacitor networks are designed to terminate 8 transmission lines using the Thevenin equivalent parallel termination technique. Again, a 0.1 µF capacitor is provided to help maintain a solid Vee level within the package, mitigating any potential cross talk or feedthrough effects. The 803 is designed for use with 10K ECL whereas the 805 is designed for use with 100K ECL.

R_1 and R_2 are calculated using the following equations:
$R_2 = (V_{ee}/V_{tt})*Z_o$
$R_1 = (R_2*V_{tt})/(V_{ee}-V_{tt})$

For a 10K ECL supply voltage of -5.2V and V_{tt} of -2V:
$R_2 = 2.6*Z_o$
$R_1 = R_2/1.6$

For a 100K ECL supply voltage of -4.5V and V_{tt} of -2V:
$R_2 = 2.25*Z_o$
$R_1 = R_2/1.25$



Thevenin Equivalent Parallel Termination Technique

References:

1. Blood, W.R., MECL System Design Handbook, Motorola, Inc., 1983.
2. F100K ECL Data Book, Fairchild Semiconductor Corp., 1986.
3. MECL Device Data, Motorola, Inc., 1987.
4. ECLinPS Data, Motorola, Inc., 1987.