Device Mounting Technology

Surface Mount Technology
Surface mounting is still the most common and economical approach for many applications. Bourns® Microelectronic Module products offer the latest in surface mount technology:

- Chip sizes to 0201
- SOIC, PLCC, TSOP, QFP to 0.012 ” (0.3 mm)
- CSP, odd form components
- BGA: 0.5 mm pitch, underfill
- Inert reflow
- Lead free solder capability
- Passive component test

Chip & Wire/COB (Chip on Board)
This proven technology provides an intermediate level of miniaturization, the advantages of in-process test and repair, and is designed to withstand harsh environments such as automotive applications. Bourns® Microelectronic Module products offer the latest in chip & wire technology:

- Gold & Aluminum Wire Bonding - High speed, automated, ball/wedge, wedge/wedge, ribbon
- Gold Wire Bonding - 20-50 µm (0.8 to 2 mil) wire to 80 µm (3.2 mil) pitch
- Aluminum Wedge Bonding - 125-380 µm (5 to 15 mil) wire for high current/power applications
- Die Attachment - Epoxy or Eutectic, 5 µm accuracy, glob top, dam & fill

Flip Chip Mounting
This process provides the ultimate opportunity for package miniaturization and minimization of conductor lengths and size reduction in high speed, high frequency applications. Bourns® Microelectronic Module products offer a choice of flip chip approaches:

Full Process for Stud Bump Bonding
**Anisotropic Adhesive Attachment**  
*(Z-axis conductive epoxy)*  
- Ideal for PCB and flex circuits  
- High I/O  
- Tight pitch  
- Cost-effective flip chip solution  
- Utilizes off-the-shelf wire bondable ICs

**Stud Bump bonding**  
- Ideal for high I/O flip chip to ceramic substrate  
- Mid-process replacement of faulty chips  
- Underfill required  
- Proven technology with reliability data  
- Utilizes off-the-shelf wire bondable ICs

**Thermal-Sonic Bonding (Gold-to-Gold Interconnect)**  
- Ideal for high frequency applications and MEMs to ceramic substrates  
- I/O limited to ~32 or less  
- Underfill optional  
- Low temp process  
- Lead free

**Solder Mounting**  
- Standard flip chip technology  
- Solder bumped devices  
- Optional underfill  
- Z-axis control for ultimate strength  
- High volume cost-effective solution

**Choice of Package Interconnects**  
- CSP (Chip Scale Packaging) – smallest package for surface mounting  
- MCM (Multichip modules) – smallest package for multichip hybrid

- SIP (Single Inline Packaging) – 0.050 " , 0.100 " and 1.8 mm  
- DIP (Dual Inline Packaging) – 0.100 "  
- BGA (Ball Grid Array)  
- QFP (Quad Flat Pack)  
- J-Leads in Dual or Quad configuration – 0.050 " , 0.075 " and 0.100 "  
- Mini-DIL  
- TO-cans  
- Butterfly  
- Hermetic Seal
Thick Film Multilayer

**Substrate Materials**
- **Alumina (Al₂O₃) Ceramic**
  - 94 %, 96 % and 99.6 % Alumina content available.
  - High level of heat dissipation (20 W/m K).
- **Aluminum Nitride (AlN)**
  - Highest level of heat dissipation (up to 200 W/m K) without the toxic effects of BeO.
  - Coefficient of thermal expansion closely matching silicon.
  - Superior reliability for applications that require a high level of temperature cycling.

**Conductive Through-Holes**
- Multiple conductor materials available to coat, plug, or fill through-holes in the ceramic substrate. *(Figure1)*
- Multiple through-hole diameters and high density through-hole arrays are available.
- Edge wraps and castellation features are also available.

**Conductors**
- Multiple conductor materials available to allow for wire bonding, soldering, and brazing (Au, Ag, Pt and PdAg).
- Available conductor thickness from 4 to 25 microns.
- Fine line conductors available with .001 " feature width and spacing. *(Figure2)*
  - Integrated microwave features are available: filters, inductors, microstrips and Lange couplers.
  - Cost reduction by converting thin film circuits to thick film.

**Dielectrics**
- **Printed Dielectric:**
  - Multiple dielectric constants available (K=6-12 standard, K=4 available).
  - Via resolution of .008 ".
  - Also used for crossovers, solder stops, and protective coatings.
- **Photo Imaged Dielectric:**
  - Dielectric constant K=8-10.
  - High density multilayer interconnects with via resolution of .002 ".
**Integrated Passive Components**

- **Thick Film Resistors (Figure 3)**
  - Resistance values available from 1 ohm/sq to 10M ohm/sq.
  - TCR of 50 ppm is available.
  - As fired tolerance of ± 20 %, laser trimmed values to ± 1 %.
  - Automated active laser trim available.

- **Thick Film Capacitors (Figure 4)**
  - Dielectric constant from K=20 to K=1500 available.
  - Laser trimmed values to 5 %.

**Other Multilayer Options Available from Bourns, Inc:**

- **LTCC (Low Temp. Co-Fired Ceramic) & HTCC (High Temp. Co-Fired Ceramic)**
  - Extremely high interconnect density utilizing multiple laminated layers.
  - Coefficient of thermal expansion matched to semiconductor die for flip chip attachments.
  - Good thermal conductivity for power application.

- **Organic Substrates**
  - FR4, FR5, Polyimide, Flex, etc.

*For any requirements outside the scope of these specifications, please contact your local Bourns representative.*

Please contact your local Bourns Sales Representative for more information.

**Americas:**
- Tel +1-951 781-5500
- Fax +1-951 781-5700

**Europe:**
- Tel +41-(0)41 768 55 55
- Fax +41-(0)41 768 55 10

**Asia-Pacific:**
- Tel +886-2 256 241 17
- Fax +886-2 256 241 16