### General Information

The 2FAD-C20R devices, manufactured using Thin Film On Silicon technology provide ESD protection and EMI filtering for the data port of portable electronic devices such as cell phones, modems and PDAs. The device incorporates six low pass filter channels. Each channel has a series 100 ohm resistor assuring a minimum of -30 dB attenuation from 800 MHz to 3 GHz. The device is suitable for EMI filtering of GSM, CDMA, W-CDMA, WLAN and Bluetooth frequencies.

Each external port of the six channels includes a back-to-back 6.5 Volt Zener diode for ESD protection. Two additional standalone 6.5 Volt Zener diodes are available for ESD protection on power lines or USB data ports. The ESD protection provided by the component enables an eight line data port to withstand a minimum ±8 KV Contact / ±15 KV Air Discharge when tested according to the ESD method specified in IEC 61000-4-2. The device measures 2.04 mm x 2.64 mm and is available in a 20 pin (4 x 5 array) CSP package intended to be mounted directly onto an FR4 printed circuit board. The CSP device meets typical thermal cycle and bend test specifications without the use of an underfill material.

### Electrical & Thermal Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Zener Diode</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Breakdown Voltage @ 1 mA</td>
<td>$V_{BR}$</td>
<td>6</td>
<td>7.2</td>
<td>8</td>
<td>V</td>
</tr>
<tr>
<td>Leakage Current @ 3 V</td>
<td>$I_L$</td>
<td>1</td>
<td></td>
<td></td>
<td>uA</td>
</tr>
<tr>
<td><strong>ESD Performance (Note 1 &amp; 2)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Withstand: Contact Discharge</td>
<td>±8</td>
<td></td>
<td></td>
<td></td>
<td>kV</td>
</tr>
<tr>
<td>Withstand: Air Discharge</td>
<td>±15</td>
<td></td>
<td></td>
<td></td>
<td>kV</td>
</tr>
<tr>
<td>Let Through: Contact Discharge</td>
<td>±150</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Let Through: Air Discharge</td>
<td>±150</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>Channel Specification</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resistance</td>
<td>$R$</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>Ω</td>
</tr>
<tr>
<td>Capacitance @ 1 V &amp; 1 MHz</td>
<td>$C$</td>
<td>50</td>
<td>55</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Filter Attenuation: 800 MHz – 3000 MHz</td>
<td>-30</td>
<td>-40</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td><strong>Thermal Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>$T_J$</td>
<td>-40</td>
<td>25</td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$T_{S}$</td>
<td>-60</td>
<td>25</td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td>Total Power Dissipation @ 70 °C</td>
<td>$P_D$</td>
<td></td>
<td></td>
<td>100</td>
<td>mW</td>
</tr>
</tbody>
</table>

**Note:**
1. The IEC 61000-4-2 test method will be adapted for component level testing. The device will provide the specified ESD protection performance on the “EXT1 – EXT8” pins only.
2. “Let Through” is a measure of the component of an incident ESD transient that the protection device allows through to the downstream circuitry.

Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.
**2FAD-C20R Series - Integrated Passive & Active Device using CSP**

### Mechanical Characteristics

This is a Silicon-based device and is packaged using chip scale packaging technology. Solder bumps, formed on the Silicon die, provide the interconnect medium from die to PCB. The bumps are arranged on the die in a regular grid formation. The grid pitch is 0.5 mm and the dimensions for the CSP packaged device are shown in Fig. 2 below.

![Device Mechanical Drawing](image)

### Reliability

Reliability data exists and continues to be gathered on an ongoing basis for Bourns Integrated Passive and Active Devices using CSP packaging.

“Package level” testing of the integrity of the solder joint is carried out on an independent Daisy-Chain test device. A 25-Pin Daisy Chain component is available from Bourns for this purpose. (Part No: 2TAD-C25R) This is a 5 x 5 array, featuring 0.5 mm pitch solder bumps. The Distance to Neutral Point (DNP) on that component is larger than that of the 2FAD-C20R and is thus deemed a worse case for Thermal Cycle testing.

“Silicon level” reliability performance will be assured by similarity to other integrated passive CSP devices from Bourns.

### Individual Channel Schematic

This section contains the schematic (See Fig. 3 below) for the single channel in the integrated passive device. Note that the electrical parameters of primary interest are (a) DC Resistance (b) ESD performance and (c) low pass filter attenuation. In terms of DC parameters it should be noted that all resistor values have a tolerance of ±10 %. This schematic consists of a series 100 ohm resistance and two Back to Back Zener 6.5 Volt diodes for ESD protection.

![Channel Schematic](image)

**Key Design Parameters**
- Source Impedance: 50 Ω
- Load Impedance: 50 Ω
- DC Channel Resistance: 100 Ω ±10 %
- Channel Capacitance: 55 pF Max @ 1 V & 1 MHz
- $V_{BR}$: 6 V Min, 8 V Max @ $I_{BR} = 1$ mA.
- $I_{IS}$: 1 μA Max @ $V_R = 3$ V
- Filter Attenuation: -30 dB Minimum @ 800 MHz - 3000 MHz
2FAD-C20R Series - Integrated Passive & Active Device using CSP

Block Diagram

Figure 4 contains a block diagram of the CSP device. This diagram includes the pin names and basic electrical connections associated with each channel.

Marking

The device will be laser marked on the backside according to the following Fig. 5 scheme below. Position A1, on the Bump Grid is located at the top left of the die when the die is orientated so that the mark is read in the normal fashion.

Fig. 4 – Device Block Diagram

Fig. 5 – Backside Laser Mark

PCB Design and SMT Processing

Please consult Bourns' Thin Film on Silicon using CSP Users Guide Application Note for notes on PCB design and SMT processing.

2FAD-C20R Frequency Response

-20
-40
-60
1 MHz
700 MHz
3 GHz
50 dB
-50 dB
34 dB
1.0 MHz
10 MHz
100 MHz
1.0 GHz
5.0 GHz

How to Order

- Thinfilm
- Model
- Chipscale
- No. of Solder Bumps
- Packaging Option
  - R = Tape and Reel
  - Packaged 3000 pcs / 7 "reel
- Terminations
  - LF = Sn/Ag/Cu (lead free)
  - Blank = Sn/Pb

Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.
Device Pin Out

The Pin-Out for the device is shown in Fig. 6. Note also that the device is shown with bumps facing up.

![Diagram of Device Pin Out]

<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Out</th>
<th>Function</th>
<th>Pin Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXT2</td>
<td>A1</td>
<td>INT1</td>
<td>C1</td>
</tr>
<tr>
<td>EXT3</td>
<td>A2</td>
<td>Ground</td>
<td>C2</td>
</tr>
<tr>
<td>EXT4</td>
<td>A3</td>
<td>Ground</td>
<td>C3</td>
</tr>
<tr>
<td>EXT5</td>
<td>A4</td>
<td>Ground</td>
<td>C4</td>
</tr>
<tr>
<td>EXT6</td>
<td>A5</td>
<td>EXT8</td>
<td>C5</td>
</tr>
<tr>
<td>EXT1</td>
<td>B1</td>
<td>INT2</td>
<td>D1</td>
</tr>
<tr>
<td>Ground</td>
<td>B2</td>
<td>INT3</td>
<td>D2</td>
</tr>
<tr>
<td>Ground</td>
<td>B3</td>
<td>INT4</td>
<td>D3</td>
</tr>
<tr>
<td>Ground</td>
<td>B4</td>
<td>INT5</td>
<td>D4</td>
</tr>
<tr>
<td>EXT7</td>
<td>B5</td>
<td>INT6</td>
<td>D5</td>
</tr>
</tbody>
</table>

Packaging

The product will be dispensed in an 8 mm x 4 mm Tape and Reel format - see Fig. 7 diagram below. The Tape and Reel package will conform to customer specification.

![Diagram of Tape and Reel Packaging]

Specifications are subject to change without notice. Customers should verify actual device performance in their specific applications.

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