



TISP7350H3SLL

**TRIPLE ELEMENT
BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTOR**

TISP7350H3SLL Overvoltage Protector

Simultaneous 500 A 2/10 GR-1089-CORE Rating

Simultaneous 100 A 10/1000 GR-1089-CORE Rating

Ion-Implanted Breakdown Region
- Precise and Stable Voltage

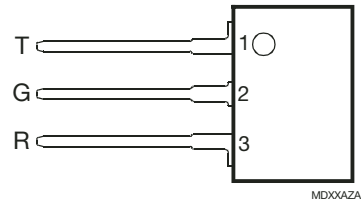
Low Voltage Overshoot Under Surge

Device Name	V _{DRM} V	V _(BO) V
TISP7350H3SLL	275	350

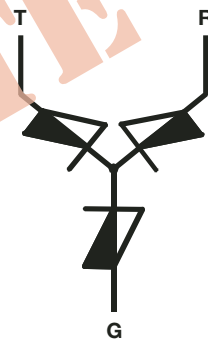
Rated for International Surge Wave Shapes
- Single and Simultaneous Impulses

Wave Shape	Standard	I _{PPSM} A
2/10	GR-1089-CORE	500
8/20	IEC 61000-4-5	350
10/160	TIA-968-A	250
10/700	TIA-968-A	200
10/560	ITU-T K.20/21	130
10/1000	GR-1089-CORE	100

3-SIP (Long Lead) Package (Top View)



Device Symbol



SD-TISP7-001-a

.....UL Recognized Component

Description

The TISP7350H3SLL limits overvoltages between the telephone line Ring and Tip conductors and Ground. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line.

Each terminal pair, T-G, R-G and T-R, has a symmetrical voltage-triggered bidirectional thyristor protection characteristic. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage onstate. This low-voltage on-state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current helps prevent d.c. latching as the diverted current subsides.

These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and matched breakover control and are virtually transparent to the system in normal operation. They are designed to voltage limit and withstand the listed international lightning surges in both polarities.

How to Order

Device	Package	Carrier	Order As	Marking Code	Std. Qty.
TISP7350H3SLL	3-SIP (Long Lead)	Tape & Ammo Pack	TISP7350H3SLLAS	SP7350H3	2000
		Tube	TISP7350H3SLL-S		1000

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
FEBRUARY 2005 - REVISED MAY 2007
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

TISP7350H3SLL Overtoltage Protector

BOURNS®

Absolute Maximum Ratings, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage (see Note 1)	V_{DRM}	± 275	V
Non-repetitive peak impulse current (see Notes 2 and 3) 2/10 μs (GR-1089-CORE, 2/10 μs voltage wave shape) 8/20 μs (IEC 61000-4-5, 1.2/50 μs voltage wave shape, 8/20 current combination wave generator) 10/160 μs (TIA-968-A, 10/160 μs voltage wave shape) 4/250 μs (ITU-T K.20/21, 10/700 μs voltage waveshape, dual) 0.2/310 μs (CNET I 31-24, 0.5/700 μs voltage waveshape) 5/310 μs (ITU-T K.20/21, 10/700 μs voltage wave shape, single) 5/320 μs (TIA-968-A, 9/720 μs voltage wave shape) 10/560 μs (TIA-968-A, 10/560 μs voltage wave shape) 10/1000 μs (GR-1089-CORE, 10/1000 μs voltage wave shape)	I_{PPSM}	± 500 ± 350 ± 250 ± 225 ± 200 ± 200 ± 200 ± 130 ± 100	A
Non-repetitive peak on-state current (see Notes 2, 3 and 4) 20 ms, 50 Hz (full sine wave) 16.7 ms 60 Hz (full sine wave) 1000 s, 50 Hz a.c.	I_{TSM}	55 60 0.9	A
Initial rate of rise of on-state current, exponential current ramp, maximum ramp value $< 200\text{ A}$	di_{T}/dt	400	A/ μs
Junction temperature	T_{J}	-40 to +150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-65 to +150	$^\circ\text{C}$

- NOTES: 1. Derate value at $-0.13\text{ }^\circ\text{C}$ for ambient temperatures below $25\text{ }^\circ\text{C}$.
 2. Initially the device must be in thermal equilibrium with $T_{\text{J}} = 25\text{ }^\circ\text{C}$.
 3. These non-repetitive rated currents are peak values of either polarity. The rated current values may be applied to any terminal pair. Additionally, both R and T terminals may have their rated current values applied simultaneously (in this case the G terminal return current will be the sum of the currents applied to the R and T terminals). The surge may be repeated after the device returns to its initial conditions.
 4. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. Derate current values at $-0.61\text{ }^\circ\text{C}$ for ambient temperatures above $25\text{ }^\circ\text{C}$.

Electrical Characteristics for any Terminal Pair, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DRM} Repetitive peak off-state current	$V_{\text{D}} = V_{\text{DRM}}$ $T_A = 25\text{ }^\circ\text{C}$ $T_A = 85\text{ }^\circ\text{C}$			± 5 ± 10	μA
$V_{(\text{BO})}$ Breakover voltage	$dv/dt = \pm 750\text{ V/ms}$, $R_{\text{SOURCE}} = 300\ \Omega$			± 350	V
$V_{(\text{BO})}$ Impulse breakover voltage	$dv/dt \leq \pm 1000\text{ V}/\mu\text{s}$, Linear voltage ramp, Maximum ramp value = $\pm 500\text{ V}$ $di/dt = \pm 20\text{ A}/\mu\text{s}$, Linear current ramp, Maximum ramp value = $\pm 10\text{ A}$			± 362	V
$I_{(\text{BO})}$ Breakover current	$dv/dt = \pm 750\text{ V/ms}$, $R_{\text{SOURCE}} = 300\ \Omega$	± 100		± 800	mA
V_{T} On-state voltage	$I_{\text{T}} = \pm 5\text{ A}$, $t_{\text{W}} = 100\ \mu\text{s}$			± 5	V
I_{H} Holding current	$I_{\text{T}} = \pm 5\text{ A}$, $di/dt = \pm 30\text{ mA/ms}$	± 150		± 600	mA
dv/dt Critical rate of rise of off-state voltage	Linear voltage ramp, maximum ramp value $< 0.85V_{\text{DRM}}$	± 5			kV/ μs
I_{D} Off-state current	$V_{\text{D}} = \pm 50\text{ V}$ $T_A = 85\text{ }^\circ\text{C}$			± 10	μA
C_{O} Off-state capacitance	$f = 1\text{ MHz}$, $V_{\text{d}} = 1\text{ V rms}$, $V_{\text{D}} = 0\text{ V}$ $f = 1\text{ MHz}$, $V_{\text{d}} = 1\text{ V rms}$, $V_{\text{D}} = -1\text{ V}$ $f = 1\text{ MHz}$, $V_{\text{d}} = 1\text{ V rms}$, $V_{\text{D}} = -2\text{ V}$ $f = 1\text{ MHz}$, $V_{\text{d}} = 1\text{ V rms}$, $V_{\text{D}} = -50\text{ V}$ $f = 1\text{ MHz}$, $V_{\text{d}} = 1\text{ V rms}$, $V_{\text{D}} = -100\text{ V}$			84 67 62 28 26	pF

TISP7350H3SLL Overvoltage Protector

BOURNS®

Thermal Characteristics, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$ Junction to ambient thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM}(1000)$ (see Note 5)			50	$^\circ\text{C/W}$

NOTE: 5. EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information

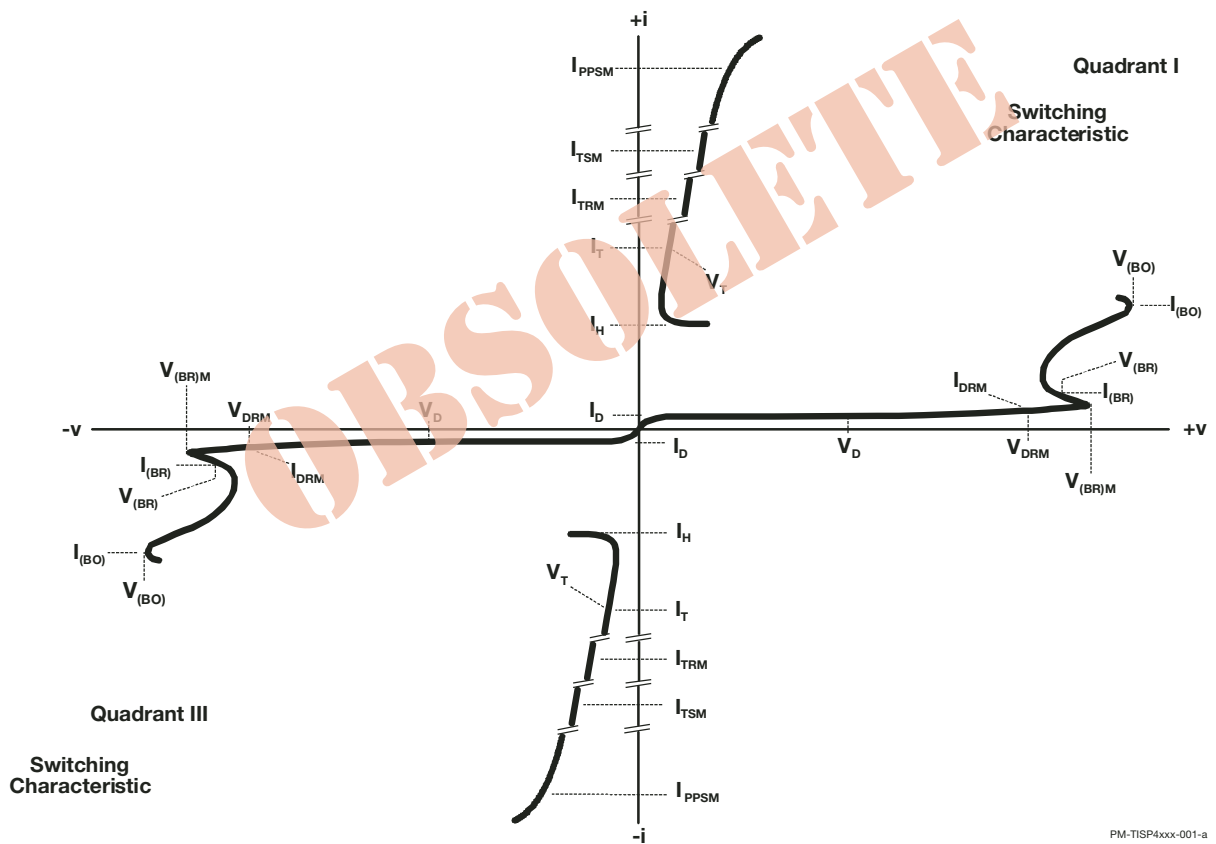


Figure 1. Voltage-Current Characteristic for Terminal Pairs

PM-TISP4xxx-001-a

Bourns Sales Offices

Region	Phone	Fax
The Americas:	+1-951-781-5500	+1-951-781-5700
Europe:	+41-41-7685555	+41-41-7685510
Asia-Pacific:	+886-2-25624117	+886-2-25624116

Technical Assistance

Region	Phone	Fax
The Americas:	+1-951-781-5500	+1-951-781-5700
Europe:	+41-41-7685555	+41-41-7685510
Asia-Pacific:	+886-2-25624117	+886-2-25624116

www.bourns.com

Bourns® products are available through an extensive network of manufacturer's representatives, agents and distributors. To obtain technical applications assistance, a quotation, or to place an order, contact a Bourns representative in your area.



Reliable Electronic Solutions