BOURNS®

Overcoming Creepage and Clearance Constraints with Bourns® PTVS1 and PTVS2 DFN Series

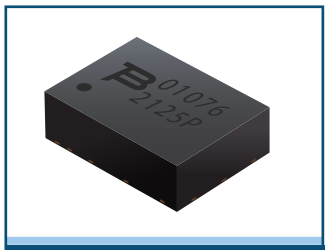
WHITE PAPER

Author: Thomas Tran, R&D & Test Manager, Bourns, Inc.
Co-Author: Lizzett Tapia, Jr. Marketing Engineer, Bourns, Inc.
Technical Contact: Protection Division Engineering, Bourns, Inc. — americus@bourns.com

Introduction

This white paper addresses a specific question facing engineers evaluating compact surge protection devices: Can a small DFN package meet the creepage and clearance requirements defined by UL 840 and IEC 60664-1? Using the Bourns® PTVS1-XXXC-H and PTVS2-XXXC-H DFN series as a reference, this paper explains how material selection, package geometry, and PCB layout together enable compliance without compromising surge performance.

Creepage and clearance compliance is not determined by package size alone. IEC 60664-1 and UL 840 implement a performance-based approach called insulation coordination, which sets required spacing based on the material comparative tracking index (CTI), the operating environment (pollution degree), and the transient overvoltage category. Each of these factors can be specified and controlled in a compact DFN design.



Bourns® Model PTVS1-XXXC-H

Bourns® Model PTVS2-XXXC-H

The result is that a properly designed 8 mm × 6 mm surface-mount package can meet the same safety requirements that once drove designers toward large through-hole formats—while also improving surge-clamping performance.

Why Large Packages Create Electrical Problems

Historically, engineers addressed creepage and clearance requirements by selecting physically large packages, TO-247, TO-220, SMC, and similar formats, to create visible air and surface distances between high-voltage nodes. That approach works from a spacing standpoint, but it introduces two electrical problems that worsen as transient rise times decrease.

Inductance adds to clamping voltage. Long leads and elevated packages add several nanohenries of parasitic inductance (L) to the surge current path. During a fast-rising surge event, this inductance generates a voltage spike governed by:

$$V_{total} = V_{clamp} + \left(L \times \frac{di}{dt}\right)$$

This (L × di/dt) component can exceed the protected load's breakdown voltage before the TVS diode turns on. The larger and taller the package, the more inductance it adds, and the less protection margin remains for downstream silicon.

Large packages disrupt PCB layout. TO-247 and similar through-hole components interrupt ground planes, force longer trace runs and increase overall system impedance. These effects compound the parasitic inductance problem and can reduce the protection margin that the TVS diode is intended to provide.

Eliminating long leads resolves both problems. The PTVS1 and PTVS2 DFN packages mount flush to the board surface with terminations on the bottom, reducing parasitic inductance to near zero. The (L × di/dt) voltage addition is effectively removed, allowing the diode to clamp surges more tightly to the protected rail than a leaded or elevated package can at the same clamping-voltage rating.

BOURNS®

Overcoming Creepage and Clearance Constraints with Bourns® PTVS1 and PTVS2 DFN Series

WHITE PAPER

Insulation Coordination: The Compliance Framework

Compliance with UL 840 and its international equivalent IEC 60664-1 is not a function of physical package size. Both standards implement an insulation coordination system that determines the required creepage and clearance distances based on a combination of factors, each of which can be specified and controlled in a DFN-based design.

A. Material Comparative Tracking Index (CTI)

CTI measures a material's resistance to surface tracking—the formation of conductive carbon paths under sustained electrical stress and contamination. UL 840 and IEC 60664-1 define four material groups based on CTI:

- Group I: CTI ≥ 600
- Group II: 400 ≤ CTI < 600
- Group IIIa: 175 ≤ CTI < 400
- Group IIIb: 100 ≤ CTI < 175

Higher CTI ratings permit shorter minimum creepage distances at a given voltage and pollution degree. The PTVS1 and PTVS2 DFN series use a molding compound classified as Material Group I (CTI ≥ 600)—the highest-rated category under UL 840 and IEC 60664-1. When evaluated in a properly designed PCB assembly, this material classification supports compliance with applicable creepage requirements using smaller physical distances than would be required for lower-CTI materials.

B. Pollution Degree

IEC 60664-1 and UL 840 characterize the operating environment by the degree of pollution, which reflects the presence of conductive contaminants—such as dust, moisture, or condensation—that may reduce the effectiveness of surface insulation.

- **Pollution Degree 1**: No pollution, or only dry non-conductive pollution. Applies to sealed or conformal-coated assemblies. Under these conditions, the allowable creepage distance drops sharply.
- **Pollution Degree 2:** Typical of most industrial and controlled commercial environments. Only non-conductive pollution is expected, with occasional temporary conductivity from condensation. This is the default assumption for most industrial PCB assemblies.
- **Pollution Degree 3:** Conductive pollution is present, or non-conductive pollution may become conductive due to condensation. Applies to uncontrolled outdoor or harsh industrial environments.

This guidance is provided specifically for basic insulation requirements. In pollution degree 2 conditions, a properly designed PTVS1 or PTVS2 DFN footprint meets the applicable minimum creepage requirements. In pollution degree 1 conditions, such as when conformal coating is applied, the margins increase further.

C. Rated Impulse Voltage and Clearance

Clearance requirements (minimum air gap) are based on rated impulse voltage, not continuous working voltage. Because the PTVS1 and PTVS2 diodes are specifically designed to clamp transient events to predictable levels, the surrounding PCB layout can be coordinated to a lower impulse withstand category. This reduces clearance requirements across the board—not just at the TVS diode location.

Minimum creepage distances under UL 840 are determined by the combination of RMS working voltage, pollution degree, and material group. For example, at 100 V RMS under Pollution Degree 2 with Material Group I, UL 840 Table 9.1 requires a minimum creepage of 0.71 mm. At 250 V RMS under the same conditions, the requirement rises to 1.25 mm. These thresholds drop sharply under Pollution Degree 1 conditions and decrease further when Material Group I compounds are specified.

Overcoming Creepage and Clearance Constraints with Bourns® PTVS1 and PTVS2 DFN Series

WHITE PAPER

PTVS1 and PTVS2 DFN Series: Package Design and Compliance

Both the PTVS1-XXXC-H and PTVS2-XXXC-H are packaged in the same 8.0 mm × 6.0 mm × 2.5 mm DFN format. The PTVS1 is rated for 1 kA peak surge current (8/20 µs per IEC 61000-4-5); the PTVS2 is rated for 2 kA. Both offer bidirectional protection across eight standoff voltage options from 22 V to 86 V, carry UL recognition (File No. E215609), and are RoHS-compliant and halogen-free.

Package Geometry

The anode and cathode terminations are located on the bottom of the package, on opposite sides of the 8.0 mm dimension. There are no leads, no elevated body, and no through-hole clearances to manage.

The distance between the inner edges of the two pads on the PCB meets the minimum creepage requirements under UL 840 for the voltage ranges this device covers, particularly when a solder mask bridge is applied between the pads as described in the layout section below.

The footprint is designed to meet IPC-2221 internal conductor spacing requirements.

Flammability

The package molding compound carries a UL 94-V-0 flammability rating, confirming that the material self-extinguishes after ignition. This rating is required for most industrial and commercial end-product safety certifications.

Package Outline and Recommended Land Pattern

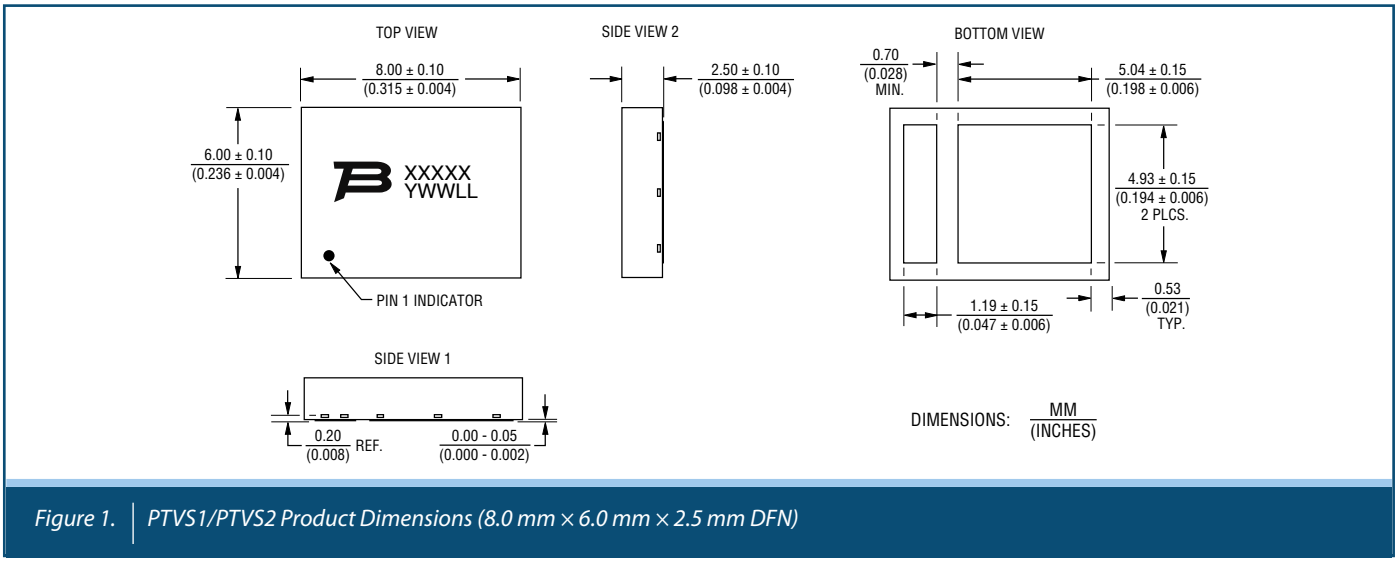


Figure 1. | PTVS1/PTVS2 Product Dimensions (8.0 mm × 6.0 mm × 2.5 mm DFN)

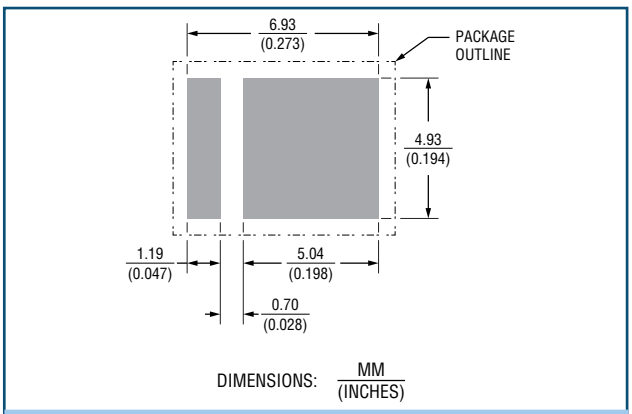


Figure 2. | PTVS1/PTVS2 Recommended Pad Layout

BOURNS®

Overcoming Creepage and Clearance Constraints with Bourns® PTVS1 and PTVS2 DFN Series

WHITE PAPER

PCB Layout Requirements

The compliance argument depends on the layout. Selecting the correct device is necessary but not sufficient; the PCB design must also meet the geometry and routing requirements below. Each rule addresses a specific failure mode.

1. Solder Mask Bridge Between Pads

Do not use a mask-defined pad for the gap between the anode and cathode terminations. Instead, apply a physical solder mask to bridge across the gap as a vertical barrier. This increases the effective surface creepage path that current must travel to arc between the two pads, directly supporting compliance with UL 840 and IEC 60664-1 creepage requirements. The solder mask bridge also reduces the risk of solder bridging between the pads during reflow.

2. Six-Via Minimum in the Ground Pad

For 1-2 kA surge exposure, a single via in the ground pad will act as a fuse. The current density through a 0.3 mm via at these surge levels exceeds what a single conductor can carry without failure. A minimum of six 0.3 mm vias distributed across the ground pad is required to distribute peak current and provide a low-impedance thermal path to internal copper layers. Fewer vias create a bottleneck that can result in failure during a surge event, removing the thermal path and compromising protection for subsequent surges.

3. Surge Path Topology

The PTVS diode must be the first component the surge current encounters on the protected line. Routing the surge current past the TVS location and then back to it through a stub creates an inductive delay in the protection path. This stub inductance reintroduces the same $L \times di/dt$ problem that the DFN package was chosen to eliminate. The TVS diode should be placed as close to the port entry point as the layout permits, with the surge current path running directly through the device before reaching any other components.

4. Reference Figure 2 for Land Pattern Dimensions

The recommended pad layout shown in Figure 2 is the reference geometry for PCB footprint design. It defines the pad dimensions, pad-to-pad spacing, and the overall land-pattern area, all of which are consistent with the package outline in Figure 1. Deviating from this layout—particularly by reducing pad-to-pad separation—may compromise both electrical performance and the creepage geometry supporting compliance.

Summary

The PTVS1 and PTVS2 DFN series satisfies creepage and clearance requirements through the combined effect of two factors: a Material Group I molding compound (CTI ≥ 600) that permits reduced minimum spacing under UL 840 and IEC 60664-1, and a PCB layout approach that extends the effective surface creepage path. No single factor is sufficient in isolation—insulation coordination requires all three to be addressed together.

At the same time, the DFN architecture eliminates the parasitic inductance that leaded and elevated packages add to the surge current path. This means switching to a DFN format does not involve a compliance-for-performance tradeoff. Designers achieve tighter clamping, a smaller PCB footprint, and equivalent safety compliance—provided the layout requirements in this document are followed.

Product Information

Bourns® Power TVS Diodes – PTVS1-XXXC-H
Bourns® Power TVS Diodes – PTVS2-XXXC-H

Next Steps

To evaluate the PTVS1 or PTVS2 DFN series for your application, download the product datasheets at the links above. For layout review support or application-specific compliance questions, contact Bourns applications engineering at:
americus@bourns.com (Americas)
eurocus@bourns.com (Europe)
asiacus@bourns.com (Asia-Pacific).