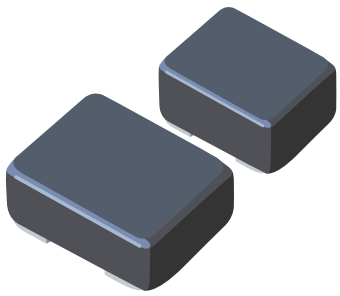
BOURNS®

Optimizing Client DDR5 Power Management Efficiency with Bourns® SRP2512CL and SRP3212CL Series Shielded Power Inductors

APPLICATION NOTE

Introduction

Client DDR5 memory is increasingly adopted in high-performance consumer devices such as laptops, desktops, and gaming systems. These systems demand higher data rates and improved power efficiency within tight space and thermal constraints.
This application note highlights how Bourns® SRP2512CL and SRP3212CL Series shielded power inductors, when paired with DDR5 Power Management Integrated Circuits (PMICs), can effectively address the power delivery challenges in Client DDR5 systems. These inductors support optimized power conversion efficiency and are designed to meet JEDEC standards for next-generation memory modules.



Bourns® SRP2512CL and SRP3212CL Series Shielded Power Inductors

Background

The DDR5 memory architecture introduces a new localized power delivery scheme, moving voltage regulation from the motherboard to the memory module. To support this, JEDEC has defined detailed specifications not only for PMICs but also for the associated inductors, including dimensions, inductance values, DCR, and ACR.

Furthermore, JEDEC mandates minimum power conversion efficiency targets for PMICs across light and heavy load conditions. As a result, the selection of high-efficiency, low-loss inductors is critical to achieving compliance and ensuring reliable DDR5 system performance.

Product / Technology Solution

In typical Client DDR5 DIMM designs, power is delivered through three separate channels—SWA, SWB, and SWC—each with distinct inductance requirements. SWA and SWB commonly use 0.47 µH inductors, while SWC uses 1.0 µH.

The Bourns® SRP2512CL and SRP3212CL Series shielded power inductors are engineered to meet the rigorous demands of such configurations. These inductors are optimized for high current handling, low losses, and compact layouts—ideal for modern DDR5 memory modules.

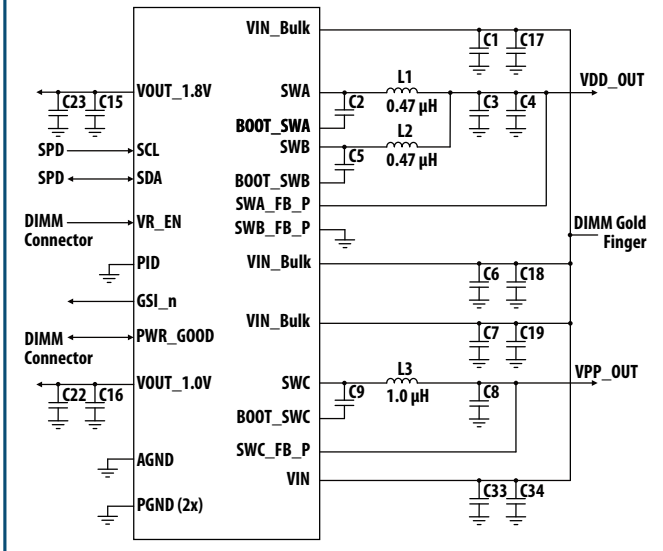


Figure 1 - Single Phase Regulator - DDR5 PMIC Schematic

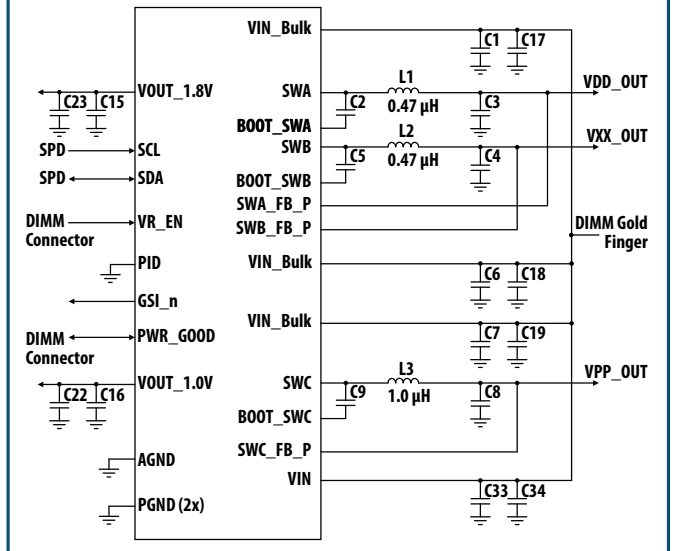


Figure 2 - Dual Phase Regulator - DDR5 DIMM Schematic

Product / Technology Solution (Continued)

Key design features include:

- **Nanocrystalline core** for high saturation current and reduced core loss, improving energy efficiency under load.
- **Low DCR and ACR** to minimize conduction losses and enhance overall power conversion.
- **Shielded construction**, which helps suppress magnetic field radiation and improves signal integrity in high-speed environments.
- **Compact SMD packaging** in 2520 and 3030 sizes, supporting layout flexibility in dense module designs.

These inductors integrate seamlessly with JEDEC-compliant DDR5 PMICs, meeting defined parameters such as size, inductance, DCR, and ACR—ensuring both compatibility and performance in client DDR5 applications.

Results and Benefits

System-level testing with DDR5 PMICs demonstrates that Bourns® SRP2512CL and SRP3212CL inductors consistently achieve power conversion efficiencies that align with JEDEC requirements.

Their optimized electrical performance—combining low DCR, low ACR, and strong current handling—helps maximize energy efficiency while supporting the compact form factors needed in Client DDR5 modules. These inductors also contribute to reduced EMI and greater design flexibility, making them a reliable choice for engineers balancing performance, space, and cost in next-generation computing systems.

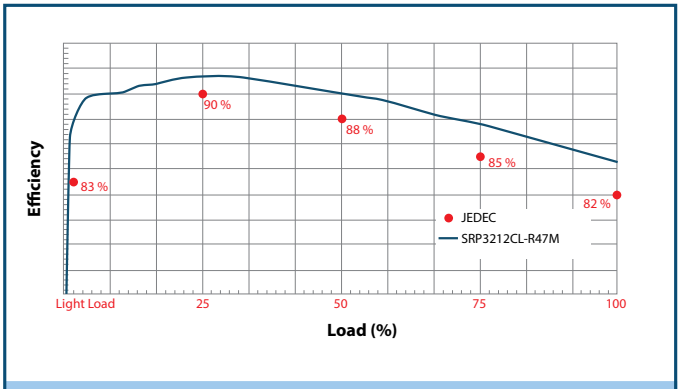


Figure 3 - Typical Efficiency Chart SWA/SWB

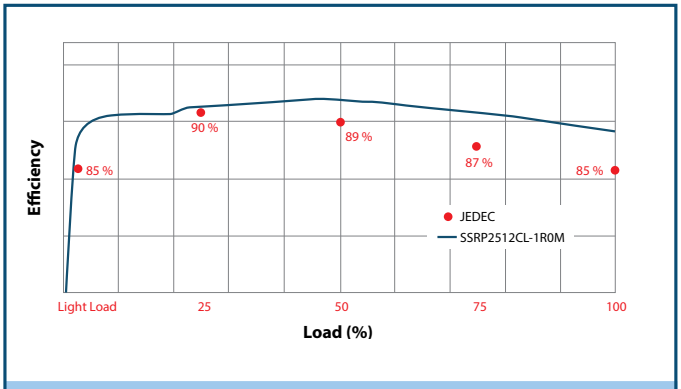


Figure 4 - Typical Efficiency Chart SWC