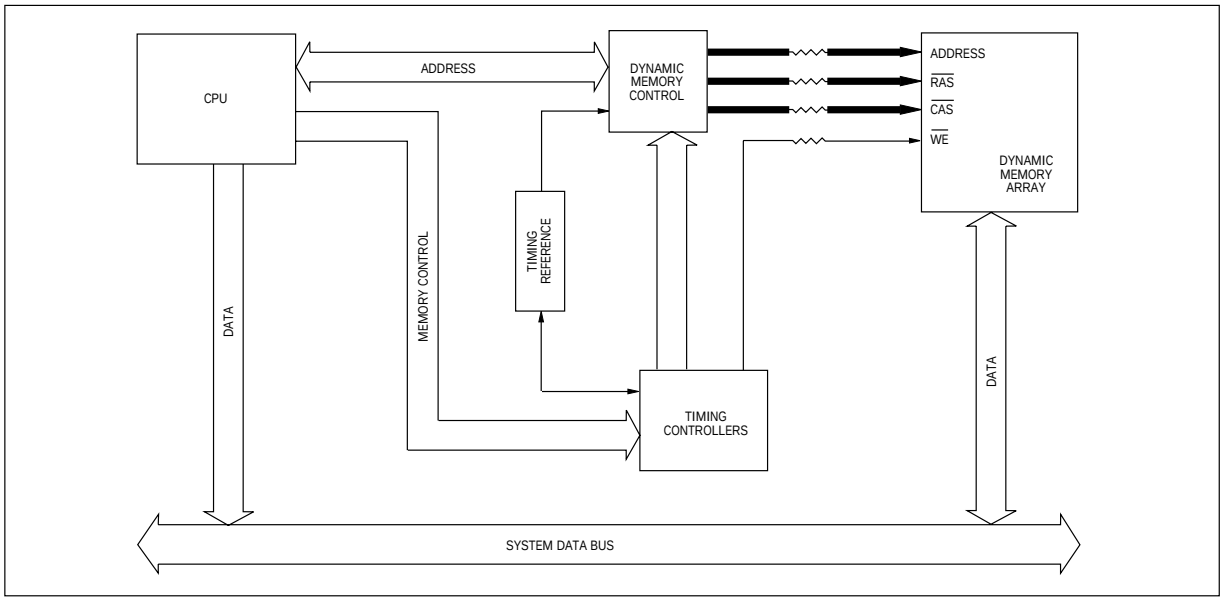
For complete product specifications, download Bourns' data sheets:

4100R Series	4400P Series	4800P Series
4300H Series	4600H Series	
4300M Series	4600M Series	
4300R Series	4600X Series	

DRAM Applications

BOURNS®



BLOCK DIAGRAM OF DRAM SYSTEM

Use Bourns Networks To:

- *Match impedance between memory driver and the DRAM array.*
- *Minimize reflections and ringing in DRAM inputs.*
- *Prevent undershoot of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals which may result in latch-up of DRAM inputs*
- *Improve system performance by allowing faster setting times for DRAM inputs.*

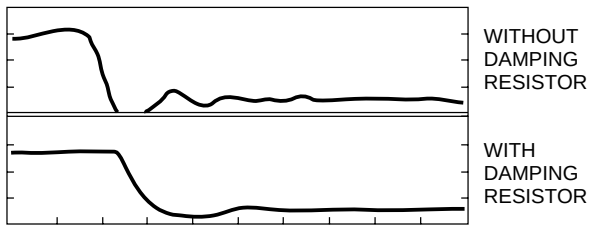
Need For Damping

The address lines ($\overline{RAS}$, $\overline{CAS}$) and control lines ($\overline{WE}$) of dynamic RAM arrays are driven in parallel, causing significant loading on the driver of the DRAM arrays. Each DRAM control input ($\overline{WE}$) has capacitive loading between 5pF to 7pF, while each address line input has about a 10pF load.

Thus each DRAM input can be modeled as a transmission line with distributed inductance and capacitance. If not properly terminated, signal reflections and ringing on the line will result, adversely affecting the performance of the memory system. The effects on signal transitions will be:

1. Increased settling time delay on low-to-high transitions.
2. Voltage undershoot on high-to-low transitions.

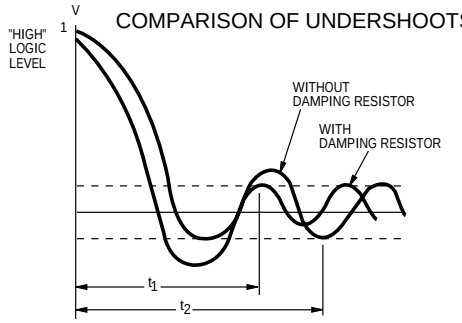
EFFECT OF DAMPING RESISTOR



Courtesy of B. Narasimhan and J. Shaffer, Micron Techology Corporation.

Increased settling time due to ringing reduces system performance because the design has to allow for the settling delay before sampling the signal. Undershoot, by bringing the input voltage below 0 volts, can damage the driver IC as well as alter the DRAM's internal address register contents, causing potential loss of data.

COMPARISON OF UNDERSHOOTS



t_1 - TIME TO ACCEPTABLE "LOW" LOGIC LEVEL FOR DRIVER WITHOUT DAMPING RESISTOR

t_2 - TIME TO ACCEPTABLE "LOW" LOGIC LEVEL WITHDAMPING RESISTOR

Application Guidelines

Termination of address and control lines is typically accomplished with low-valued resistors placed in series at the driver output. Selection of the proper resistance value is performed in two steps: approximation of the proper resistance using transmission line equations, and secondly, through trial and error, changing the resistance value to account for real world deviations such as PCB vias and bends.

The appropriate transmission line equations are as follows:

Z_o = characteristic line impedance (microstrip)

$$= \frac{87}{\sqrt{er + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \text{ ohms}$$

T_d = propagation delay of the line

$$= 1.017 \sqrt{0.475e_r + 0.67} \text{ ns/in.}$$

C_o = trace capacitance = 1000 (T_d/Z_o) pF/in.

C_d = equivalent trace capacitance associated with each DRAM. It takes 0.5 inch to interconnect one DRAM.

$$= 3.5\text{pF}/0.5 \text{ in.} = 7 \text{ pF/in.}$$

Z_o' = effective characteristic impedance, accounting for capacitive loading of the DRAMs.

$$= \frac{Zo}{\sqrt{1 + C_d/C_o}}$$

T_d' = effective propagation delay, accounting for the capacitive loading of the DRAMs

$$T_d = T_d \sqrt{1 + C_d/C_o}$$

where e_r = relative dielectric constant of the PCB's glass epoxy layer

h = distance from the trace to the ground plane

w = width of trace

t = thickness of trace

(Ref. MMI Systems Design Handbook, pp. 10-5 and 10-6.)

For example, for a trace with the following characteristics:

e_r = 5 (for G10 glass epoxy)

h = 30 mils

w = 15 mils

t = 3 mils

then, Z_o = 85 ohms

T_d = 0.15 ns/in.

C_o = 1.76 pF/in.

Z_o' = 38 ohms

T_d' = 0.35 ns/in.

Thus on a theoretical basis, the design will require the resistance of 38 ohms to match the trace impedance of the PCB.

However, the actual impedance will differ from this theoretical value due to the non-ideal characteristics of the PCB trace geometry (i.e., bends, curves and vias in the trace), as well as the manufacturing variations inherent in the components and materials. Therefore, a trial-and-error process must be employed in order to optimize the value of the damping resistor.

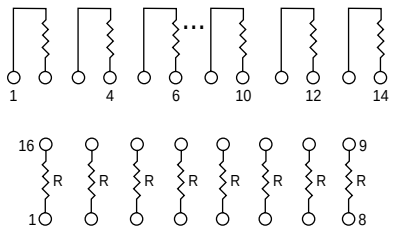
The procedure involves selecting various values around the calculated value and observing the resulting waveforms on an oscilloscope. Choose the value that best balances the reduction in ringing/reflection and the reduction in speed: a large resistance value provides better damping, but will also add delay by slowing the edge rate. Typically, resistance values for memory damping will be in the range of 10 ohms to 50 ohms, with the most common values in the 20 ohm to 30 ohm range.

Since memory damping is a type of series termination, distributed loading along the line will not be possible. That is, the entire lumped load must be located at the end of the line, with no other loads along the signal path. This will guarantee that the waveform will remain undisturbed as it travels along the line. For related reasons, the placement of the series damping resistor should be as close to the driving device as possible.

Bourns Networks For Memory Damping

Bourns can supply a wide range of standard resistor networks for memory damping applications. Standard resistance values (see below) are normally in stock. However, any intermediate value within the range 10 ohms to 10 megohms can be supplied.

The following package and pin count options are available:



NUMBER OF LINES				
	2	**3**	**4**	**5**
MSIP* CSIP* PCC	4304M-102-RC 4604X-102-RC	4306R-102-RC 4606X-102-RC	4308R-102-RC 4608X-102-RC	4310R-102-RC 4610X-102-RC 4210P-102-RC
	6			
MSIP* CSIP* PCC	4612X-102-RC			
	7	**8**	**9**	**10**
DIP CSIP* SOM SOL SOL-J PCC	4114R-1-RC 4614X-102-RC 4814P-1-RC	4116R-1-RC 4816P-1-RC 4416P-1-RC 4416J-1-RC	4118R-1-RC	4120R-1-RC 4420P-1-RC 4420J-1-RC 4420P-102-RC

*MEDIUM PROFILE (.250" SEATED HEIGHT) AND HIGH PROFILE (.350" SEATED HEIGHT) ARE AVAILABLE BY PLACING THE LETTER "M" OR "H," RESPECTIVELY, IN THE FIFTH POSITION OF THE PART NUMBER.